Delay Modelling Improvement for Low Voltage Applications

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Abstract

Based on an explicit formulation of delays, an improved model for low voltage operation of CMOS inverter has been derived. Extrinsic and intrinsic effects, such as transistor current variation, input slew rate effects and mobility improvement at low field are considered. Explicit dependence of inverter delay on input controlling ramp is given with clear evidence of supply and threshold voltage influences. Validations are obtained by comparing the calculated and measured oscillation period evolution of ring oscillators, under supply voltage conditions varying from standard 5v, to values as low as the highest threshold voltage of the process involved.

The speed performance evolution and the limits to the reduction of supply voltage are clearly given in terms of threshold voltage values.

1 Introduction

In the design of digital circuits, switching speed of the circuit is one of the important parameters to be considered. Great effort has been given to the development of accurate analytical delay models for CMOS gates. These models are useful for understanding and defining performance trade off with respect to design parameters and better use the design space. The delay of CMOS structures depends on the structural parameters (arrangement and sizes of transistors), the output load (with full layout parasitic capacitances), technology parameters, including short channel saturation effects and input wave form slopes.

If structural and loading parameters can be considered quite well with standard RC modelling, technology parameters and input slope effects are becoming more and more important for modern technologies and low voltage applications.

Sakurai [1] has recently introduced his α-power law MOSFET model to take into account the velocity saturation effects, allowing a good prediction of transition times for inverters with reasonable loads and fast varying input ramps. However low voltage modelling of modern technologies must render as well short channel than low field effects in a continuous way. Varying the supply voltage induces extrinsic effects such as current variation and input slew rate effects, and intrinsic ones on the mobility and effective transistor lengths which values can never been determined separately from test structure measurements. For that, theoretical model refinements can hardly reproduce intrinsic effects involved in average variations such as those to be considered in current evaluation for switching delay estimations. Moreover if direct influence of supply voltage on step responses of inverters or gates can be predicted quite easily, modifications induced in the input slew rate contribution to real propagation times are not yet so clearly given.

In the first delay models presented to include input slew rates [2,3], the propagation delay was written as a linear contribution of step responses characteristic of the switching inverter and of its controlling device. These models did not include the influence of short circuit currents and were limited to fast input ramps. Further improvement has been obtained in [4], where simple technology dependent corrections extend the application range of the preceding models over a large domain of configurations. Recently Jeppson [5], in an attempt to consider exact wave form and coupling capacitances obtained a physical expression equivalent to a second order development of the rationale function of [4].

As a common feature of these models, delays of inverters (gates) are increased by a significant fraction of the time spent by the controlling input ramp, to rise (fall). This is clearly shown in figure 1 which illustrates the simulated variations of the propagation delay of an inverter (with constant load), controlled by different input ramps. The fraction of input delay to be considered, has been tentatively physically defined in [4], as the time spent by the input ramp to create sufficient current unbalance in the controlled device, to equilibrate the output load (thus allowing output voltage variation). In

fact, for usual tapering factors, it has been observed that this unbalance is sufficient only when the P (or N) is completely switched off.

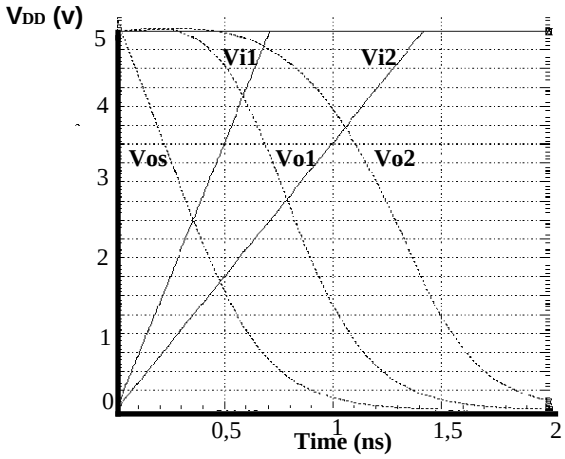

Fig. 1. Effect of input transition time on gate delay: Vos, Vo1, Vo2 represent the output response to step, and 0,7 and 1,4 ns input transition time respectively.

In that conditions, defining delays with respect to the half supply voltage and considering linear input wave forms, the input ramp contribution to the propagation delay were easily obtained as the time necessary for the input to ramp from $V_{DD}/2$ to V_{DD}-$|V_{TP}|$ or (V_{TN}) for rising (falling) input edges, such as:

$$At_{LHS}(IN) \text{ or } Bt_{HLS}(IN) \qquad (1)$$

with $A = 1 - 2\frac{|V_{TP}|}{V_{DD}}$ and $B = 1 - 2\frac{V_{TN}}{V_{DD}}$

where $t_{LHS,HLS}$ represent the step response of the controlling device.

If this delay model gives good results for standard 5v supply voltage, it appears insufficient for low voltage application and almost when the range of supply voltage approaches the sum of the threshold voltages. It has been clearly observed that gate delays increase exponentially when V_{DD} approaches $V_{TN}+|V_{TP}|$. This is due to the decrease of the current available which controls the step response and to the increase of the contribution of the input slew delay. This is illustrated in figure 2 where we show the supply voltage dependence of the dynamic transfer characteristic of an inverter with a constant load, controlled by an identically loaded inverter. As it can be observed, lower is the supply voltage value, larger is the fraction of the input ramp necessary to switch the output (ie larger is the time to create sufficient current unbalance to equilibrate the load). This trend is not reproduced using A (B) expressions in equation 1.

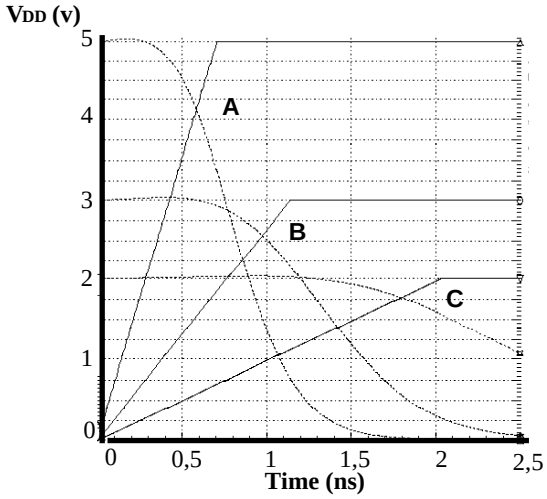

Fig. 2. Effect of supply voltage variation on the dynamic transfer characteristic: A, B, C input output curves have been obtained for V_{DD} = 5, 3 and 2v respectively.

We propose in this paper a modelling, for low values of supply voltage, of the intrinsic effects and of the input slope contribution to the delay of inverters. For that we will first study the effect of the supply voltage on the individual step responses. Then we will consider the effect of the input slew rate. Validations will be given through SPICE simulations and measurements of the supply voltage sensitivity of the oscillation period of integrated ring oscillators.

2 Low Voltage Modelling of Step Responses

We first study here the step response modifications induced by the decrease in supply voltage. In former work [6,7] we defined step responses of inverters (gates) as the average charge transfer necessary to equilibrate the output load under the input drive. This charge transfer has been understood as produced by the unbalance current developed in the cell under consideration, as:

$$t_S = \frac{C_L \Delta V}{< I >} \qquad (2)$$

where t_S is the delay evaluated at half supply voltage, C_L the total output load, ΔV the output voltage swing (here $V_{DD}/2$) and <I> the average output unbalance current.

As given in [6,7], this average current can be evaluated easily through effective parameters. This results in explicit equations for delays such as:

$$t_{HLS} = \tau_{ST}\frac{C_L}{2C_N}$$
$$t_{LHS} = \tau_{ST}R(\mu)\frac{C_L}{2C_P} \qquad (3)$$

where:

$$\tau_{ST} = \frac{L_{\min} L_{effN}}{\mu_{effN}} \frac{16 V_{DD}}{7 V_{DD}^2 - 12 V_{DD} V_{TN} + 4 V_{TN}^2} \quad (4)$$

characterises the intrinsic speed of the process, and:

$$R(\mu) = \frac{L_{effP}}{L_{effN}} \frac{\mu_{effN}}{\mu_{effP}} \frac{7 V_{DD}^2 + 4 V_{TN}^2 - 12 V_{DD} V_{TN}}{7 V_{DD}^2 + 4 V_{TP}^2 - 12 V_{DD} |V_{TP}|} \quad (5)$$

models the effective process dissymmetry between N and P transistors. L_{min} and L_{eff} represent the geometrical and electrical lengths respectively, C_N and C_P stand for the active capacitances of the switching devices. μ_{eff} correspond to the average effective mobility over the voltage swing, including saturation effects.

As shown in [8], these parameters can be obtained directly from calibrations on SPICE simulations (using foundry supplied level 6 model, for ex.) or determined directly from specific test structures implemented on ring oscillators. In this way they appear as effective parameters averaging all second order effects across the voltage swing. Their initial definition can be obtained on relatively simple Shichman and Hodges model using average values of μ and L, or in direct process calibration allowing real account of short channel effects.

These equations have been validated for supply voltage values greater than the sum of the threshold voltages ($V_{TN}+|V_{TP}|$), condition in which the transistors operate between saturation and linear mode. For V_{DD} values lower than $V_{TN}+|V_{TP}|$ and greater than V_{TN} or $|V_{TP}|$ (ie out of the sub threshold regime), the consideration of the transistor operating mode shows that they are always working in saturation mode, and the value of the average current, used in (2) must be modified. Conserving the general shape of equ.3, the parameters defined in equ.4 and 5 become:

$$\tau_{ST} = \frac{L_{\min} L_{effN}}{\mu_{effN}} \frac{2 V_{DD}}{(V_{DD} - V_{TN})^2} \quad (6)$$

$$R(\mu) = \frac{L_{effP}}{L_{effN}} \frac{\mu_{effN}}{\mu_{effP}} \frac{(V_{DD} - V_{TN})^2}{(V_{DD} - |V_{TP}|)^2}$$

Note here that further modelling for sub threshold range could be obtained in the same way, following [9]. However, as we will show later, the degradation of speed and sensitivity to process variation is so important that sub threshold operating mode does not appear very reliable for high performance digital applications.

As obtained in equ. 6, τ_{st} and $R(\mu)$ reflects the explicit dependence of the delay parameters to the supply voltage variation. To be complete it is necessary to consider the implicit dependency of the mobility. In equ. 4 and 5, the mobility values are determined at V_{DD}=5v, and after calibration on SPICE (level 6), they represent the effective value of this parameter, across the voltage swing. The decrease of V_{DD} lowers the field on the transistor channel resulting in an improvement of the effective mobility value. To model correctly low voltage effects, this improvement of the mobility must be introduced. This can be done easily considering that at very low V_{DD} the mobility value must be equal to the low field one, and at standard 5v it is decreased due to field effects in the channel. First order modelling can be obtained with the empirical expression:

$$\mu_{eff}(V_{DD}) = \frac{\mu_o}{1 + \theta(V_{DD} - V_T)} \quad (7)$$

where μ_o is the low field effect mobility and θ an empirical coefficient to be determined from the calibrated value of the mobility at V_{DD}=5v, as:

$$\theta_{N,P} = \frac{1}{(5 - V_{TN,P})} \left(\frac{\mu_{oN,P}}{\mu_{effN,P}(5v)} - 1 \right) \quad (8)$$

For a specific process, using the values of mobilities determined at 5v on test structures, it is then possible to calculate the evolution of this parameter with the supply voltage.

Results are given in fig. 3 where we compare the supply voltage variations of the measured values of the mobility to the values calculated from equ. 7. Measurements have been performed on specific ring oscillators [8] implemented on 1,2μm process (V_{TN}=0,77v, $|V_{TP}|$=1,1v). As shown, the good agreement obtained ascertains the proposed approach.

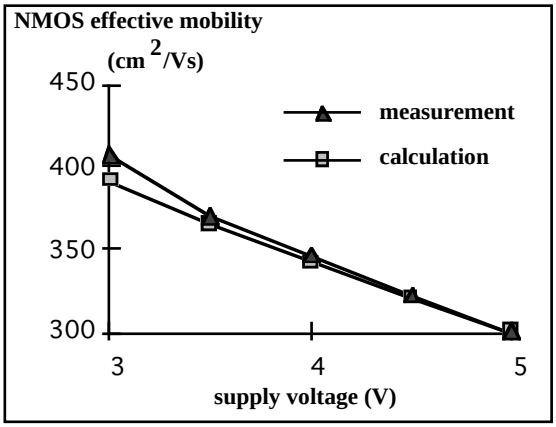

Fig. 3. Comparison of the effect of the supply voltage on the mobility: measured values have been obtained on test circuit, calculated ones from equ.7.

Table 1 illustrates the evolution of the mobility and delay parameters (equ. 4,6,7) with the supply voltage. As expected the degradation of performances is becoming prohibitive for V_{DD} values approaching the highest threshold voltage. Figure 4 highlights the sensitivity of the τ_{st} parameter to the supply voltage.

V_{DD} (v)	1.2	1.3	1.4	1.5	1.6	1.8	2	3	4	5
μ_{effN} (cm^2/Vs)	534	524	514	504	495	477	460	392	342	300
μ_{effP} (cm^2/Vs)	229	222	215	209	203	191	181	144	119	102
τ_{st} (ps)	331	241	188	153	128	97	80	45	33	28
R(μ)	44.8	17.2	10.9	8.3	7.0	5.6	4.9	3.8	3.6	3.5

Table 1: Supply voltage evolution of the mobility and delay parameters , as given from equ. 4-7

From these results we can conclude here that for $V_{DD}>V_{TN}+|V_{TP}|$ the degradation of delay performance is quite limited, the decrease of available current, due to the lowering of supply voltage, is partly compensated by the improvement of the mobility.

For $V_{DD}<V_{TN}+|V_{TP}|$ the sensitivity of the intrinsic delay performances, to the supply voltage, becomes prohibitive. Moreover, as shown in Table 1 observing R(μ) variation, the dissymmetry between N and P transistors (output falling and rising edges, respectively) is greatly affected.

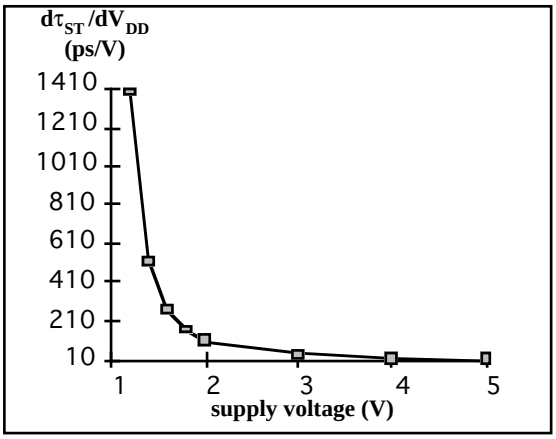

Fig. 4: Sensitivity of the intrinsic performance parameter of the process (τ_{st}) to the supply voltage variation

As a result the sum $V_{TN}+|V_{TP}|$ of the threshold voltages appears as a reasonable limit to the lowering of the supply voltage, or in other words for imposed working supply voltage, the constraint $V_{DD}/(V_{TN}+|V_{TP}|)>1$ is a good indicator for the selection of more appropriate CMOS process [10].

3 Low Voltage Input Slope Effects

Second effect to be considered in modelling supply voltage scaling is the contribution of input slew rate to real propagation delays. Input slope effects have been satisfactory introduced for "high" supply voltages by considering the time spent by the input ramp to develop sufficient unbalance current in the structure. For 5v supply voltage and fast input ramp satisfactory results were obtained by imposing total current unbalance, resulting in:

$$t_{HL}(i) = At_{LHS}(i-1) + t_{HLS}(i)$$
$$t_{LH}(i) = Bt_{HLS}(i-1) + t_{LHS}(i) \quad (9)$$

for the fall (rise) time of an inverter (i), controlled by the preceding $(i\text{-}1)^{th}$, where S subscript specifies step responses which model input, output slopes [6,7].

A and B coefficients, previously defined, represent the fraction of input ramp necessary to switch off N or P transistor block. At a lower value of the supply voltage these expressions of A and B (equ.1) predict less influence of input slew rates, in complete contradiction with the simulation results.

Let us now establish an equivalent formulation of the input slew rate contribution to the delay, useful for low supply voltage values. As specified above, we model each step response through an average unbalance current, <I>, calculated from the working mode of the switching transistor involved. We define now by I_{switch}, the unbalance current available in the inverter at the beginning of the output voltage variation. For a given process, the ratio:

$$\gamma = \frac{I_{switch}}{<I>} \quad (10)$$

is a characteristic of the structure, it represents the relative value of minimal charge necessary to modify the output (level of charge of the output capacitance).

The value of this ratio can be calculated at V_{DD}=5v. <I> has been already calculated in equ. 3 and I_{switch} is the saturation current of the ON transistor at the cut off of its complementary counterpart.

For example, evaluation for 1,2μm process gives γ=0,6. The meaning of this result is that the modification of the output is noticeable (the output begins to fall or rise) when the current available in the ON transistor represent 60% of the average current available in the ON transistor.

Let us define by $V_{INswitch}$ the value of the input ramp level satisfying this condition. At this value the ON

transistor is always saturated, which determines the value of I_{switch}. The former A (B) coefficient becomes:

$$A(B) = \frac{V_{INswitch} - V_{DD}/2}{V_{DD}/2} \quad (11)$$

where $V_{INswitch}$ is obtained from equ. 10 as:

$$\frac{1}{2}\mu_{effN,P}(V_{DD})C_{ox}\left(\frac{W}{L}\right)_{N,P}(V_{INswitch} - V_{TN,P})^2 = \gamma < I > \quad (12)$$

Considering, firstly, identical values of the threshold voltages and the previously defined value of γ, equ. 11 can be evaluated for different supply voltage values as:

$$A = 2\left[\frac{V_T}{V_{DD}} + 0,275\sqrt{4\left(\frac{V_T}{V_{DD}}\right)^2 - 12\frac{V_T}{V_{DD}} + 7}\right] - 1 \quad (13)$$

for $V_{DD} > 2V_T$ and:

$$A = 0,44\frac{V_T}{V_{DD}} + 0,56 \quad (14)$$

for $V_{DD} < 2V_T$.

The values obtained for the A coefficient are illustrated in figure 5, for supply voltage scaling from $5V_T$ to V_T. As expected from SPICE simulations, A (B) coefficient increases at lower V_{DD} values.

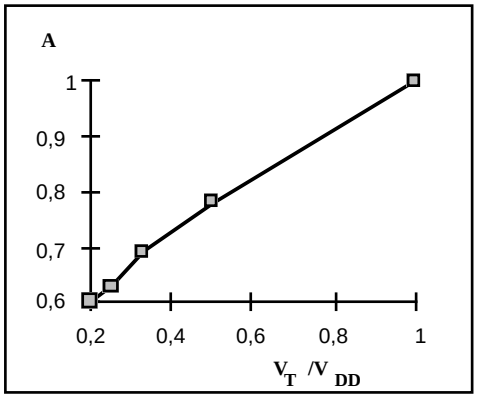

Fig. 5: Supply voltage evolution of the input slew rate contribution to the inverter delay

Considering for example, an inverter array, we can conclude that the propagation delay of the i^{th} inverter is increased by 60% of the step response of the controlling $(i-1)^{th}$ inverter, at $V_{DD}=5V_T$, and by 100% at $V_{DD}=V_T$.

After some tedious but not difficult calculation, A coefficient, for real process ($V_{TN} \pm |V_{TP}|$), can be obtained in the same way as:

$$A = 2\left[v_{tp} + \left(4v_{tn} - v_{tp}\right)\sqrt{\frac{7 + 4v_{tp}^2 - 12v_{tp}}{175v_{tp}^2 + 4v_{tp} - 60v_{tp}v_{tn}}}\right] - 1$$

for $V_{DD} > V_{TN} + |V_{TP}|$ and: (15)

$$A = 2\left[v_{tp} + \left(4v_{tn} - v_{tp}\right)\sqrt{\frac{8}{175v_{tp}^2 + 4v_{tp} - 60v_{tn}v_{tp}}\left(1 - v_{tp}\right)}\right] - 1$$

for $V_{DD} < V_{TN} + |V_{TP}|$, where $v_{tn} = V_{TN}/V_{DD}$ and $v_{tp} = |V_{TP}|/V_{DD}$ are the normalized with respect to V_{DD} threshold voltage values. The B coefficient for falling edge can be obtained easily by direct permutation of v_{tn} and v_{tp}.

Table 2 gives the variation with the supply voltage of A and B coefficients, calculated for 1,2µm process with V_{TN}=0,77v and $|V_{TP}|$=1,1v.

Validation of these results has been performed by measuring the evolution, with the supply voltage, of the oscillation period of ring oscillators integrated in 1,2µm process.

In Table 3 we compare measured periods to simulated values (HSPICE level 6) and calculated ones, using equ. 3, 9 and 15. As shown in the table, for supply voltage values ranging from 5v to 1,5v the agreement obtained between measured, calculated and simulated values is very good.

For values lower than 1,5v, the discrepancy observed is not significant because of the large sensitivity of the period to threshold voltage fluctuations when V_{DD} approaches V_T [11]. A small 5% dispersion on the threshold voltage values (which correspond to a realistic dispersion figure) can afford for the difference observed between the low voltage simulated values of the oscillation period and the real ones, measured on the ring oscillator. Moreover, for supply voltage values near the transistor threshold voltage, insufficient modelling of sub threshold effects does not permit accurate comparison. Note that V_{DD}=1,2v is a very drastic biasing condition for circuits, resulting in an important decrease of performances.

Figure 6 illustrates the supply voltage variation (in log scale) of the measured oscillation period together with the calculated values. As shown, the agreement observed between measured and calculated values, using appropriate low voltage expressions for A (equ. 15), μ_{eff} (equ. 7,8)and τ_{st} and R(µ) (equ. 6), is quite good and validates the low voltage corrections proposed here.

V_{DD}	1,2	1,3	1,4	1,5	1,6	1,8	2	3	4	5
$\lvert V_{TP}\rvert/V_{DD}$	0,917	0,846	0,786	0,733	0,687	0,611	0,55	0,367	0,275	0,22
V_{TN}/V_{DD}	0,642	0,592	0,55	0,513	0,481	0,428	0,385	0,257	0,192	0,154
A	0,96	0,92	0,89	0,86	0,83	0,79	0,76	0,66	0,59	0,55
B	0,86	0,84	0,82	0,81	0,80	0,77	0,75	0,67	0,63	0,61

Table 2: Supply voltage evolution of the input slew rate contribution to the inverter delay

V_{DD} (v)	1.2	1.3	1.4	1.5	1.6	1.8	2	3	4	5
T (ns) calculation	27397	8738	4795	3221	2400	1573	1188	559	387	317
T (ns) simulation	19100	8074	4925	3495	2691	1831	1382	630	424	331
T (ns) measurement	32735	11377	6028	3822	2824	1830	1337	579	389	307

Table 3: Calculated, simulated and measured supply voltage evolution of the oscillation period

The calculation using A (B) parameters given in equ. 1, and uncorrected parameters τ_{st} and R(μ), results in an great underestimation of performance degradation.

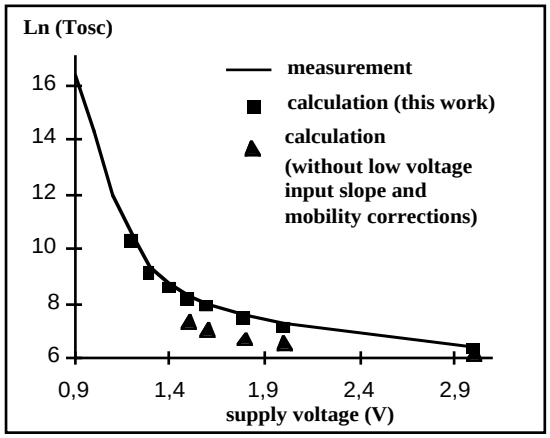

Fig. 6: Illustration of the supply voltage evolution of the ring oscillator period.

Note that for V_{DD}<1,2v, the great degradation measured may give indication of the appearance of the sub threshold operating mode of the transistors [12].

4 Conclusion

Reduction of the supply voltage is a direct consequence of CMOS technology scaling [13]. The increasing demand for reduced power dissipation while maintaining high speed operation imposes good management of the performance trade-offs. So there is a need for circuit performance prediction at low voltage.

We have presented in this paper an improvement of a former delay modelling, for low voltage operation. Considering explicit equation of delays, for inverters, we have shown how supply voltage effects can be modelled through the intrinsic speed factor (τ_{st}) and the effective dissymmetry (R(μ)) of the process, and by correct modelling of input slopes effects in delays. Calibration of effective mobility parameters on test structures appeared sufficient to give clear evidence of the delay sensitivity to the supply voltage. Limits of supply voltage reduction have been defined in terms of process parameters (transistor threshold voltages). Supply voltage sensitivity of the inverter performances has been clearly set up.

Explicit contribution of the input slew rate to the delay has been defined. Validations on measured performances of integrated test circuits have been obtained. They constitute one direct proof of modelling efficiency. Considering [6], that structural factors are not affected by low voltage operation, extension to gates is straightforward, test circuits are under development on available submicronic processes.

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