SENSAT – a Practical Tool for Estimation of the IC Layout Sensitivity to Spot Defects*

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Shorts and opens caused by spot defects may result in significant yield loss in manufacturing of VLSI circuits. Traditionally a layout design is considered correct and manufacturable if it does not contain any violations of the geometric design rules. However, it is well known that two different layouts of the same integrated circuit may exhibit different sensitivities to spot defects despite the fact that both are free from design rule violations and both occupy the same area. Therefore, a tool for verification of sensitivity to spot defects and estimation of spot defect related yield losses would be very helpful in optimization of an IC design from the viewpoint of manufacturability.

This work starts from the discussion of the relationship between occurrence of a spot defect and the circuit failure. Since a *bridge* between two separate conducting regions is not equivalent to a *short* in the circuit, and a *break* in a conducting layer is not equivalent to an *open connection*, no geometrical analysis of a single mask can provide exact estimation of the mask sensitivity to spot defect related shorts and opens. In the general case such an estimation requires understanding of the operation of the circuit. We introduce the concept of the *sensitive area* defined as the area containing the centers of all defects of a given radius *R* which result in *bridges* (or *breaks*). The sensitive area is not identical with the critical area. The critical area, as defined by others [1,2], is the area containing the centers of all defects of a given radius *R* which result in malfunction of the circuit. We say that a region in an IC mask is *sensitive* but not *critical* if defects with centers located in this region create bridges or breaks which do not affect operation of the circuit. It is possible to extract from a single mask its sensitive area but not its critical area. If the sensitive area is extracted and displayed, the designer may ignore some parts of it if he or she knows that they are not critical. As a result, a practical tool for IC layout optimization which is based on the concept of sensitive area must be interactive. SENSAT is such a tool.

Since reduction of the layout sensitivity to shorts may increase its sensitivity to opens and vice versa, a practical tool must determine sensitive areas for both. The main function of SENSAT is to extract and display the sensitive areas in the IC masks. Crucial algorithms in SENSAT are the algorithms which determine shapes of the sensitive areas for shorts and opens in the actual layout. In this work we focus our attention on the sensitive area for opens. We demonstrate that in the case of arbitrary mask geometry there are qualitative differences between the concepts of the sensitive areas for shorts and for opens, and a more complex algorithm is needed to find the sensitive areas for opens. We propose such an algorithm. This algorithm has been implemented in SENSAT together with a known algorithm [3] which determines the sensitive areas for shorts. A practical example of optimization of an analog CMOS cell layout shows how our tool can be used to reduce the sensitivity of a layout to spot defects. After redesign of metal 1 and metal 2 masks the yield limited by opens for a chip containing 1000 cells increased from 23.6 % to 29.3 %. This corresponds to 24% more good chips from a wafer. These numbers include yield losses due to defects in all masks, not only the metal masks. Therefore there is still possibility for further layout optimization.

Implementations of SENSAT exist for SUN Sparc workstations and personal computers.

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References

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