A Layout Approach to Monolithic Microwave IC

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Abstract— A layout approach is attempted dedicatedly for MMICs (Monolithic Microwave Integrated Circuits), on which predominant layout elements are transistors, resistors, capacitors, inductors, coplanar-waveguides, T-junctions, etc., formed by the GaAs fabrication process. The layout issue typical of such MMICs consists essentially in how to realize a single layer placement of different shapes of layout elements under a variety of spacing, orientating, and shaping constraints.

In this paper, each layout element is modeled to simplify placement tasks subject to different placement constraints, and then a set of the interconnection requirements among elements is represented by a graph, to which a planarization algorithm is effectively applied. As the result of this planarization, a placement procedure is constructed mainly by repeated application of a merging scheme. A number of experimental results are also shown to demonstrate the practicability of the described layout approach.

I. Introduction

With the recent advance of the GaAs IC technology, practical demands for the MMIC (Monolithic Microwave Integrated Circuit) implementation are growing rapidly, especially in the field of satellite TV broadcasting and mobile data communication (frequency band; 1-12 GHz). Hence the design productivity has to be enhanced for those MMICs which are used dedicatedly for transmitting and receiving facilities of the broadcasting/communication. However, MMICs have various aspects of refusing the design automation, as pointed out below.

The layout design of MMICs differs from that of ordinary silicon VLSIs mainly in that

(i) two metal layers, called *topside* and *bottomside* layers, are used in such a way that the former is prior to the latter, that is, the bottomside layer should be used only when a pair of layout elements can not be placed on the topside layer without overlapping,

(ii) two types of interconnection wires are necessary, one for the frequency band of 10-12 GHz and the other for that of 1-3 GHz (*remark*; in Japan frequency bands 1-3 GHz and 10-12 GHz are commercially available), and

(iii) there are too many varieties of layout constraints to facilitate the layout automation, that is, in order to realize necessary performances, not only spacing and orientating but also shaping constraints are imposed differently on each layout element, which have prevented us from attempting the layout automation.

Thus the layout design of such MMICs demands a skilled balance between handling of complexity and achievement of circuit performance. In terms of managing the complexity, of fundamental importance is how the layout process is structured so that the art and the science can be organically combined. The main reason why the layout design of MMICs has been set aside for trial-and-error type manual tasks, even although the demands for the layout automation for MMICs are growing radically, may be reduced to ill structured layout processes so far attempted.

Motivated by these situations, the present paper attempts an approach to the layout automation intended for MMICs. First, each layout element is modeled to simplify placement tasks subject to a specific set of layout constraints. Second, a set of interconnection requirements among elements is represented by a graph, to which a planarization algorithm [1,2] is effectively applied. Finally, on the basis of this planarization, a placement procedure is executed constructively by repeated application of a merging scheme to a pair of the layout blocks so far attained. A part of experimental results is also shown to demonstrate the practicability of the described layout approach.

II. Modeling of Layout Elements

The layout design of MMICs consists in the placement of layout elements with the use of two metal layers (topside and bottomside layers), as illustrated in Fig. 1 which shows a typical example obtained by manual lay-

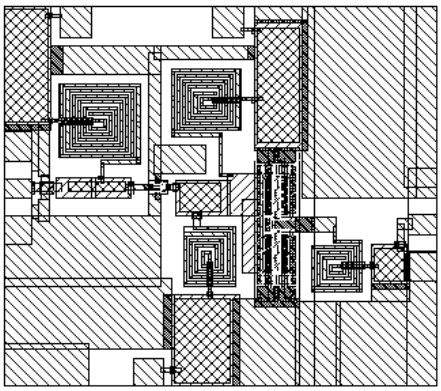


Fig. 1. Layout example obtained by manual design.

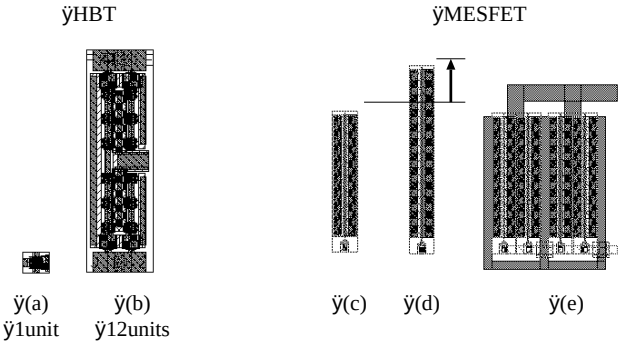


Fig. 2. Layout patterns of HBT and MESFET.

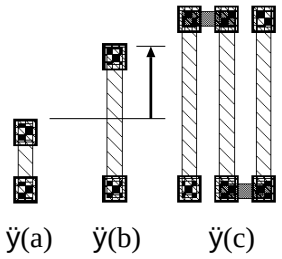


Fig. 3. Layout patterns of resistor.

out. The layout elements used for MMICs are classified into two; one is a class of circuit elements and the other is that of interconnection elements. The former consists of transistors, resistors, capacitors, inductors, and sources/grounds, and the latter of coplanar-waveguides, metal lines, T(Tee)-junctions, cross-junctions, contacts, and pads; each with different layout constraints [3].

A number of layout concepts have been devised for analog VLSIs [4–8], which may be applied to MMICs. However, the MMIC layout is different from the analog layout essentially in respect of

(i) the dynamic variation in the shape of transistors and resistors, and
(ii) the wiring junction by means of T- and cross-junctions.

Such a distinction gives rise to a main factor of interrupting the layout automation for MMICs. Thus the layout elements are modeled especially in terms of simplifying layout tasks.

[i] Transistors

There are two kinds of transistors; one is HBT (Heterojunction Bipolar Transistor), and the other MESFET (MEtal Semiconductor Field Effect Transistor). The layout patterns of an HBT are prescribed, as illustrated in Fig. 2(a) and (b), such that both the width and the height are discretely varied according to specifications. On the other hand, the patterns of an MESFET can be drawn, as exemplified in Fig. 2(c)-(d), such that according to specifications, the length in the vertical direction can be continuously variable, but the width should be discretely determined in accordance with the number of iterations. In addition, both of the HBT and MESFET of Fig. 2 can be not only reflected but also rotated by 180 degrees, whereas the rotation of ± 90 degrees is prohibited.

[ii] Resistors

The layout patterns of a resistor are exemplified in Fig. 3. The vertical length of a resistor can be continuously variable, but the width should be discrete in accordance with the number of iterations. Moreover, both the reflection and the rotation of 180 degrees are possible, but not for the rotation of ± 90 degrees.

[iii] Capacitors

A capacitor is of MIM (Metal-Insulator-Metal) type, which is composed of two metals on the topside and bottomside layers and an insulator. Their shapes should be the same rectangle with the variable aspect ratio, the area (i.e. height × width) of which is determined according to the element value. A pair of terminals are placed on the same edge or on different ones without overlapping such that one is on the topside layer, and the other on the bottom one, as shown in Fig. 4. In addition, the rotation of ± 90 as well as 180 degrees is possible.

[iv] Inductor

An inductor is in the shape of a square spiral as shown in Fig. 5, which is composed of a wire of a fixed width formed on the topside layer. The total wire length is determined

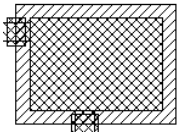


Fig. 4. Layout patterns of capacitor.

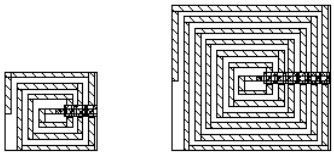


Fig. 5. Layout patterns of inductor.

by the element value. The terminal in the center of the square is formed on the bottomside layer, and the other on the topside layer. In addition, the rotation of ± 90 as well as 180 degrees is possible.

[v] Ground

A GND (GrouND) is a metal in a rectangular shape, which is formed on the topside layer. An interconnection of a number of GNDs can be admitted to costitute a single GND in a polygon shape. The rotation of ± 90 as well as 180 degrees is possible.

[vi] Metal line

A metal line is used for wiring dedicated to the frequency band of 1-3 GHz, which is formed on the topside layer. The width of a metal line is determined according to the frequency to be used. A metal line can be not only rotated ± 90 and 180 degrees but also bent 90 degrees.

[vii] Coplanar-waveguide

A coplanar-waveguide is composed of a strip-line and associated with it a pair of GNDs on both sides, as illustrated in Fig. 6. Let W be the width of a strip-line, let G be the minimum width of a GND, and let S be the minimum separation between the strip-line and GND, as shown, and we can suppose that a coplanar-waveguide has the minimum width $W + 2G + 2S$. In addition, a coplanar-waveguide can be not only rotated by ± 90 and 180 degrees but also bent by ± 90 degrees.

[viii] T-junctions and cross-junctions

A T-junction and a cross-junction are composed of metals in the shape of a letter T and a cross, respectively, formed

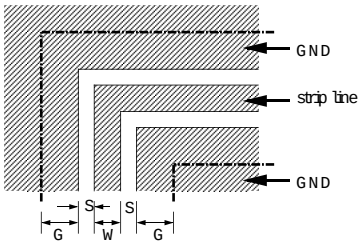


Fig. 6. Layout patterns of coplanar-waveguide.

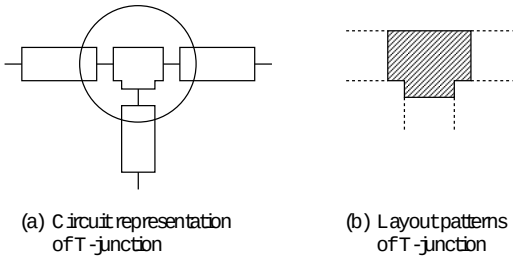


Fig. 7. T-junction.

on the topside layer, which are used for interconnection of three and four layout elements, respectively (for example, see Fig. 7).

[ix] Pad

A pad is a metal in the shape of a rectangle, which is formed on the topside layer. Pads are placed on the edges of a MMIC chip in prescribed or unprescribed order, which are used for inputs/outputs of the MMIC.

[x] Contact

A contact is a via hole in the shape of rectangle, which is used for interconnection between the topside and bottomside layers.

III. Planarization

In the fabrication process of MMICs, whenever the metalization on the bottomside layer is necessary, a bottomside metal has to be kept thinner than the topside one for the flatness of a chip, and hence usually the resistivity of a bottomside metal is much higher than that of a topside one. In order to maintain the performance on gain/noise, the priority rule has to be set down such that the bottomside layer should not be used unless a pair of layout elements can not be placed without overlapping.

Hence, given a circuit schematic to be implemented on an MMIC chip, the layout process must start with the

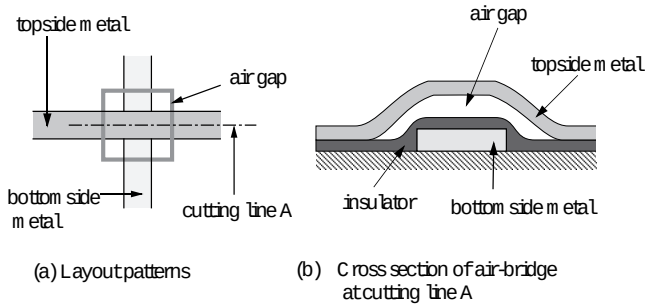


Fig. 8. Air-bridge crossover.

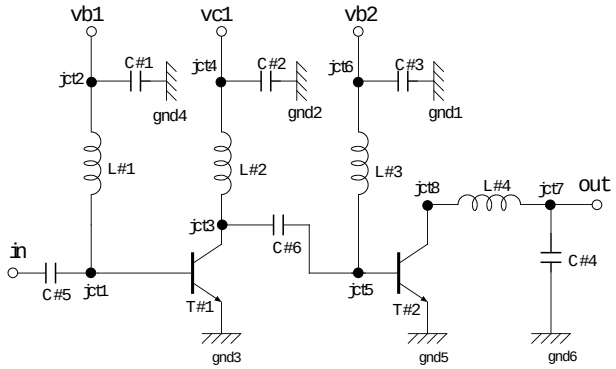


Fig. 9. MMIC schematic S.

planarization of the schematic. If the schematic can not be planar, a number of crossovers are inevitable, which are usually implemented by the so-called "air-bridge" crossovers [3], as illustrated in Fig. 8. This implies that this planarization process has to involve the issue of how to reduce the number of crossovers [2].

A. Graph Representation of Circuit Schematics

Consider an MMIC schematic as shown in Fig. 9, where there are three types of nodes; two transistors, six capacitors, and four inductors, as summarized below;

(i) **pad nodes** denoted by circles indicate pads; i.e. nodes *in*, *out*, *vbt1*, *vbt2*, and *vc1*,

(ii) **junction nodes** denoted by black circles indicate interconnection junctions; i.e. nodes *jct1* through *jct8*, where it should be remarked that apart from others, *jct8* is a common terminal of only two elements,

(iii) **GND nodes** denoted by ground symbols indicate GNDs; i.e. nodes *gnd1* through *gnd6*,

(iv) transistors; i.e. *T#1* and *T#2*,

(v) capacitors; i.e. *C#1* through *C#6*,

(vi) inductor; i.e. *L#1* through *L#4*, and

(vii) the weight of a branch between nodes u and v indicates the maximum length of the planar-line connecting nodes u and v (for simplicity, weights are omitted in Fig. 9).

It can be seen from this example that in comparison with lumped circuits, the MMIC is distinctive in that

[I] T- and cross-junctions should be regarded as layout elements,

[II] cyclic ordering is specified occasionally for a part of or all of pads.

Thus the graph representation of an MMIC schematic is different from that of a lumped circuit schematic. In what follows, a graph representation of a given MMIC schematic is defined.

[Graph Construction Rule]

Given an MMIC schematic S, construct a graph $G = (V, E)$, where V and E are sets of *vertices* and *edges*, respectively, as follows.

Vertices

V1: !! Let PG denote a set of pad nodes and GND nodes in S, and define a vertex u of G corresponds in one-to-one to each node $u \in PG$.

V2: (i) If there is a pair of junction nodes in S which is connected by a branch (for example, *jcta* and *jctb* of Fig. 10(a)), then contract them to a single junction node (for example, $jct(ab)$ of Fig. 10(b)) unless *jcta* and *jctb* should be connected by a coplanar-waveguide.

(ii) Continue this contraction so long as possible.

(iii) Let J be a set of junction nodes in S including those obtained by contraction, and define a vertex v of G corresponding in one-to-one to each node $v \in J$.

V3: !! Let ELM denote a set of transistors, resistors, capacitors, and inductors in S, define a vertex w of G corresponding in one-to-one to each element $w \in ELM$.

Edges

E1: For each branch (u, v) in S such that $u, v \in PG \cup J$, define an edge (u, v) of G corresponding in one-to-one to branch (u, v) of S, and attach to it the weight of branch (u, v).

E2: For each element $w \in ELM$ in S, if and only if node $v \in PG \cup J$ is a terminal of element w in S, define an edge (v, w) of G, and attach to it the weight of branch connecting element w to node v in S.

For example, given an MMIC schematic S as shown in Fig. 9, we can obtain a graph representation G as drawn in Fig. 11 (for simplicity, edge weights are omitted).

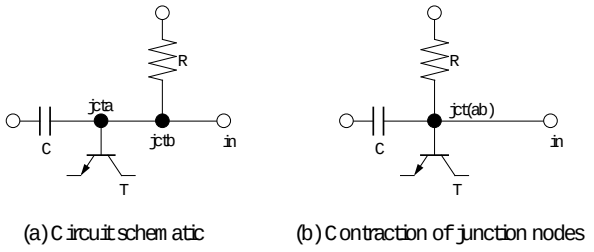


Fig. 10. Contraction of junction nodes.

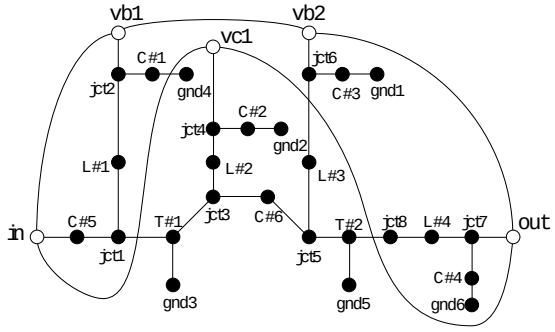


Fig. 11. Graph representation G of schematic S.

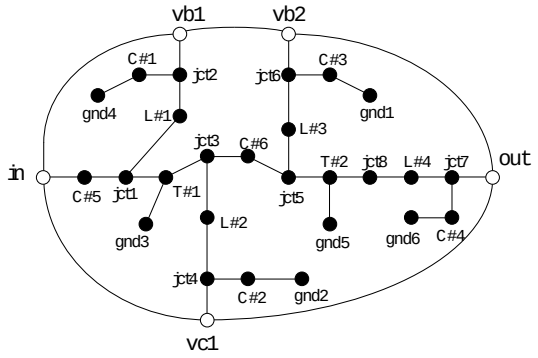


Fig. 12. Planarization of graph G of Fig.11.

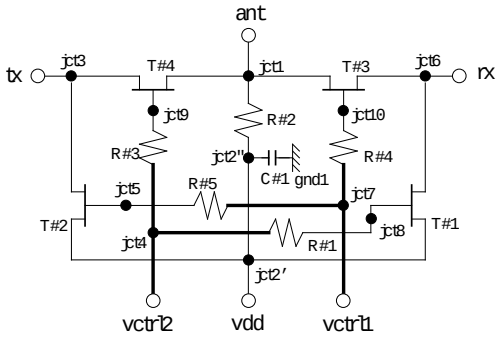


Fig. 13. MMIC schematic S' (bold lines indicate the nets admitted for crossover).

B. Planarization

In advance of planarization, we have to take it into account that we have to place layout elements only inside of a chip. In other words, let L be an enveloping contour representing the four sides of a chip, and the planarization of a graph representation G should be attempted inside of L.

Given an MMIC schematic S, let G be a graph representation of S obtained by the above construction rule. Supposing that a cyclic ordering is specified for a set of pad nodes, construct in G a loop L such that pad nodes are placed on L in the specified cyclic order. On the other hand, if no cyclic ordering is specified, then construct a loop L such that pad nodes are placed randomly on L.

As can be readily verified, if graph G can be drawn plenarily inside of L, then S proves to be realized with no crossover. For example, in the schematic S of Fig. 9, if a cyclic ordering is prescribed as (in, $vb1$, $vb2$, out, $vc1$), then a loop L is drawn accordingly as shown in Fig. 11.

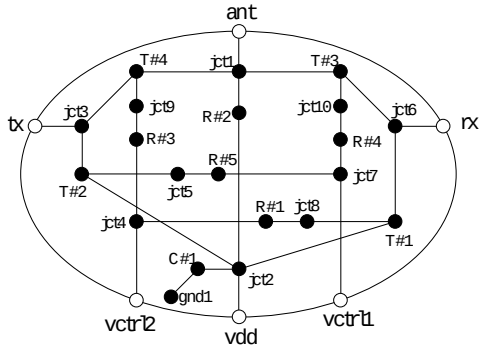
Now that we have a graph representation G with a prescribed L, we have to consider a planarization algorithm, which involves not only the planarity testing but also the planarization by deleting edges when a given graph can not be planar. As to the former, a linear time planarity testing algorithm was first discovered [1], while as to the latter, a planarization algorithm was constructed on the basis of it by means of an additional scheme of removing a minimal number of edges when a graph proves to be nonplanar [2]. Due to the limit of space, we omit the details of this planarization algorithm, but we can show a few of the implementation results below.

Fig. 12 shows a planarization of the graph G of Fig. 11. In this case, the algorithm returns the planarity of G, and then automatically draws G. On the other hand, given an MMIC schematic S' as shown in Fig. 13, a graph representation G' with a prescribed cyclic pad ordering is obtained as shown in Fig. 14(a). In this case, the algorithm returns the nonplanarity of G', and then draws a maximal planar subgraph (solid lines) by deleting edges (dotted lines), as shown in Fig. 14(b).

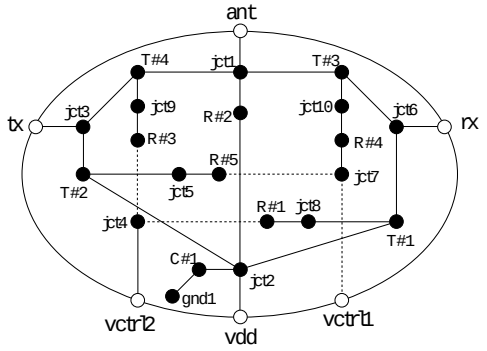
It should be added here that at the stage of removing edges from a nonplanar graph in our algorithm, edges can be selected from those admitted for crossovers.

IV. Placement Procedure

The results of the planarization contain the necessary information of placing all layout elements, such that



(a) Graph representation G'



(b) Planarization of G'

Fig. 14. Planarization of graph G'.

(i) layout elements represented by nodes and interconnections indicated by edges in the maximal planar subgraph can be realized on the topside layer, and

(ii) interconnections indicated by deleted edges in the planarization should be implemented by crossovers with the use of the bottomside.

Hence the main issue here is how to realize the physical layout on the basis of the results of the planarization process.

A. Preprocessing

Given an MMIC schematic S, a graph representation G of S is constructed exclusively for the planarization, and hence G should be reformed dedicatedly for the physical layout, as briefed below.

Step 1: Considering that all GND nodes should access to pads of a chip, add pad nodes on the contour loop L of G, whenever necessary, and connect them to GND nodes in G without destroying the planarity.

Step 2: Such a junction node j in G as is adjacent to only two nodes x and y of ELM is meaningless in the physical layout, and hence replace j together with the two edges incident to j by a single edge connecting x and y.

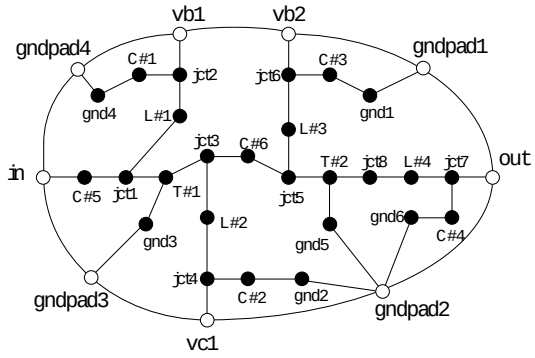


Fig. 15. Preprocessing by Step 1.

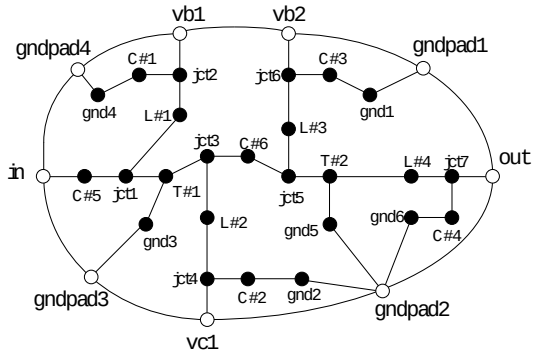


Fig. 16. Preprocessing by Step 2 and 3.

Step 3: If a junction node of degree 4 is produced in G, and the usage of a cross-junction is prohibited, then the junction node should be replaced by two junction nodes of degree 3.

For example, consider the graph G of Fig. 11. By Step 1, four pad nodes *gndpad 1-4* are added onto L to be interconnected to GND nodes, as shown in Fig. 15. By Steps 2 and 3, the graph of Fig. 15 can be reformed as shown in Fig. 16, where node *jct8* is deleted.

B. Merging Scheme

The main procedure of the physical placement consists in repeated application of a merging scheme, which is to merge a pair of layout blocks. Initially each layout element constitutes by itself a layout block, and at any stage of the merging the total shape of a layout block is restricted to a rectangle, as outlined in what follows.

Given an MMIC schematic S, we assume that for each layout element in S the following properties are satisfied.

Property 1: The total enveloping shape is a rectangle

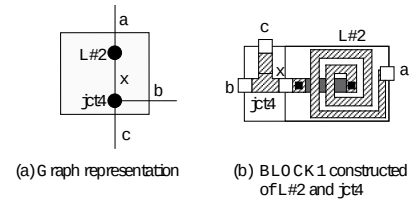


Fig. 17. Merging example for L#2 and jct4.

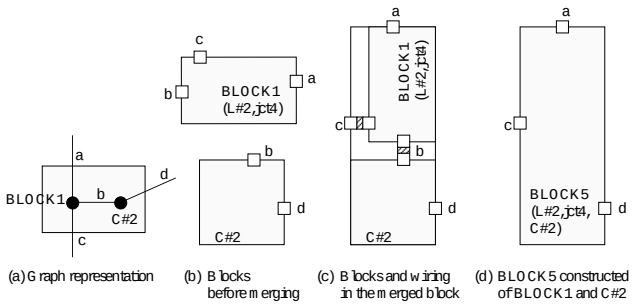


Fig. 18. Merging example for BLOCK1 and C#2.

with the prescribed sizes of height and width, whether or not the aspect ratio is variable.

Property 2: Each primary terminal to be connected to the outside is prescribed on a side of the enveloping rectangle.

Henceforth, for the easiness of exemplifying the merging process, let us use an example of the MMIC schematic S of Fig. 9 and its graph representation G of Fig. 16.

Suppose, for example, that an adjacent pair of layout elements *L#2* and *jct4* are merged into a block, denoted by *BLOCK1*, as illustrated in Fig. 17, and accordingly that vertices *L#2* and *jct4* together with an internal edge x are contracted into vertex *BLOCK1* in G, as shown in Fig. 18(a). Now, consider a pair of *BLOCK1* and *C#2*, under the assumption that the shape of *C#2* is prescribed as shown in Fig. 18(b). There are numbers of possibilities of merging *BLOCK1* and *C#2*, among which we may well select the merging of Fig. 18(c) in terms of minimizing the area of the total enveloping rectangle. Consequently, a new block, denoted by *BLOCK5*, shown in Fig. 18(d) is constructed.

This example suggests a criterion for merging an adjacent pair of layout blocks. Throughout the placement procedure, the following criterion will be set down.

[Merging Criterion]

I: The area of the total enveloping rectangle of the merged block should be minimized.

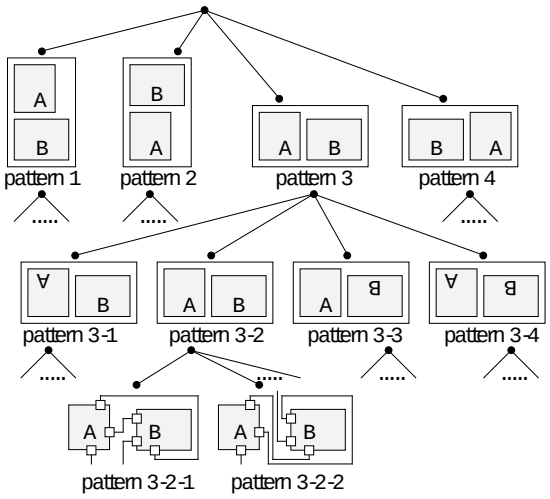


Fig. 19. Possibilities of merging.

II: The primary terminals to be connected to the outside should be on the sides of the enveloping rectangle.

It should be added here that the above criterion I is time-consuming. To see this, for example, see Fig. 19, which demonstrates possibilities of the merging.

C. Placement Procedure

In the MMIC layout, the key factor is to avoid the detouring of interconnection, since maintaining the specified performances is prior to minimizing the total chip area. Thus any algorithm so far devised for the analog layout can not be employed here, since the minimization of the chip area has been given top priority in almost all of the algorithms.

The authors have attempted so far numbers of approaches to the MMIC layout, among which the following simple procedure of repeated application of a merging scheme demonstrates the highest potential of practicability.

[Placement Procedure]

Step 0: Given an MMIC schematic S, let X be a given set of all layout elements in S.

Step 1: Construct a graph representation $G = (V, E)$ of S, and planarize G.

Step 2: Let $G_0 = (V, E_0)$ be the maximal planar subgraph of G obtained by the planarization process in Step 1.

Step 3: If $|X| = 1$, then go to Step 5, else go to Step 4.

Step 4: Select an adjacent pair of nodes $A, B \in X$ in G_0, such that the merging of A and B minimizes the

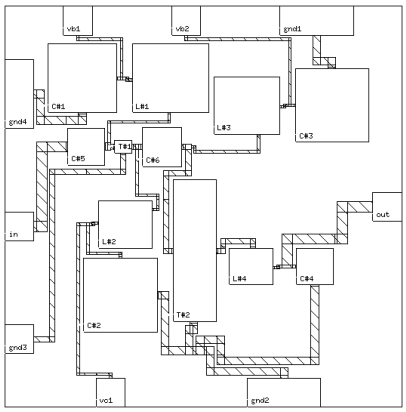


Fig. 20. Layout example obtained by our algorithm.

area of the total enveloping reactangle. Let (AB) be the merged block, and put $X \leftarrow X \cup \{(AB)\} - \{A\} - \{B\}$. Contract nodes A and B into a new node (AB) in G_0. Go to Step 3.

Step 5: Construct a crossover corresponding to each edge in $E - E_0$, and then halt.

It should be pointed out that a tuning scheme can be added to this procedure so as to improve the area efficiency, as follows:

At the stage of merging blocks A and B, attempt the tuning of the aspect ratio of either A or B (or both), provided that the aspect ratio of A or B is variable, respectively, such that the area of the total enveloping rectangle of the merged block (AB) can be minimized.

Fig. 20 shows an experimental result of our layout procedure, which is not yet completed in the sense that the physical layout of GND metals has been set aside for manual refinement.

V. Conclusion

A layout approach has been attempted dedicatedly to MMICs, which can place different shapes of layout elements under a variety of spacing, orientating, and shaping constraints.

This approach has distinctive features as

(i) a graph theoretic algorithm is adopted for planarization, and item the placement procedure is executed simply by repeated application of a merging scheme, and

(ii) the tuning of aspect ratios of elements can be inserted into the merging scheme for improving the area efficiency.

Development is continuing on tuning aspect ratios of elements, terminal positioning for elements, and refinement on GND patterns.

Acknowledgements

The authors would like to thank Professor Shuji Tsukiyama of Chuo University and Professor Toshinobu Kashiwabara of Osaka University for their constructive discussion on planarization and planar embedding of a graph with prescribed/unprescribed pads order.

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