# Current and Charge Estimation in CMOS Circuits

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**Abstract: CMOS circuits have significant amounts of dynamic short-circuit (or through) current. This can be as large as 20% of the total in well-designed circuits, and up to 80% of the total in circuits that have not been designed carefully. This current depends strongly on the relative sizes of the pull-up to pull-down paths. We introduce the *dynamic short-circuit ratio* to model this parameter. This allows accurate estimation of currents including the dynamic short-circuit current, and also results in improved delay estimation. Accuracy is typically within 10% of circuit-level simulation while operating at the switch-level abstraction**.

## 1 Introduction

Power, current and noise effects are increasingly becoming significant as fabrication technologies scale down in the deep submicron region. Emergence of low power applications is also forcing designers to be concerned about power consumption as well as its effects in circuits. There is thus an increasing need for CAD tools to help in the design and analysis of circuit that consume low power and have low noise effects.

Power consumption in CMOS circuits is affected by several interacting effects. There are three principal components that contribute to the total current in CMOS circuits. These are the capacitive current (charging/discharging of capacitance), dynamic short-circuit (or through) current due to establishment of a transient short-circuit between power and ground when a complementary gate switches, and static short-circuit current when a non-transient path between power and ground is established. Previous work [1] in this area has noted the importance of the dynamic short-circuit current, which is almost 20% of the total current in well-designed circuits and can be larger than the capacitive current in circuits that have not been carefully designed. Static short-circuit is usually not expected in CMOS circuits but our experience with real designs show that there can be significant static short-circuit current in CMOS circuits. This usually happens when delays in a circuit cause overlap between signals that are not supposed to be active simultaneously, for example, the pre-charge phase and the subsequent discharge phase. These kinds of problems in circuits are not manifest in logic-level errors and can be difficult to identify. Nevertheless, they lead to increased power consumption and noise levels that can be eliminated fairly easily when identified.

Current and charge drawn in CMOS circuits is affected by three well-known circuit parameters: input signal rise/fall time (referred to as slew from now on), load capacitance and driver size [2] [3]. In [2] and [3] these three parameters were lumped into a single parameter called the *rise-time ratio*. The rise-time ratio, or even the three parameters slew, load capacitance and driver size are insufficient to model the current and charge in CMOS circuits. We present characterization data to show that there is a fourth parameter called the ***dynamic short-circuit ratio*** ($\boldsymbol{r_{dsc}}$) that strongly affects current and charge independently of the three parameters used so far. In particular, the dynamic short-circuit current $I_{dsc}$ is a strong function of the dynamic short-circuit ratio. Intuitively, $I_{dsc}$ should be a function of the resistance of the path from power to ground formed during a dynamic short-circuit.

The dynamic short-circuit ratio is the ratio of the resistance of the pull-up (pull-down) to the resistance of the pull-down (pull-up) path for a high (low) going transition. By explicitly modelling this parameter, we are able to significantly improve accuracy of all estimated quantities. This includes not only current and charge, but also delay. Data presented in this paper shows that $I_{dsc}$ can be as large as 80% of the total current and can vary over a wide range. Also, the total charge drawn is affected by the dynamic short-circuit ratio. Thus, if we hold the input slew, load capacitance and driver size constant and only change $\boldsymbol{r_{dsc}}$ the charge can vary by as much as 20%. Most of this variation is due to $I_{dsc}$. Such effects cannot be modelled accurately without the dynamic short-circuit ratio. Ignoring the dynamic short-circuit ratio, as has been done till now, leads to significant inaccuracies.

Combining the input slew, load capacitance and driver size into a single parameter like the rise-time ratio also introduces significant inaccuracies. This is true because the effects of each of these parameters are not exactly complementary. For example, doubling the input slew does not have the same effect on the current or charge as halving the output delay even though the rise-time ratio is roughly the same in these two cases.

Utilizing the dynamic short-circuit ratio allows our algorithm to obtain results that are typically within 10% of circuit-level simulation while operating at the switch-level abstraction; this is true for the total current as well as for the dynamic short-circuit component. We are thus able to obtain performance improvements of more than three orders of magnitude over a SPICE algorithm.

The ability to explicitly estimate all three components of current, namely dynamic short-circuit, static and capacitive currents, allow us to identify and diagnose parts of the circuit that may be drawing excessive current both in the absolute and relative sense. Presence of static short-circuit current in CMOS circuits is usually due to design or timing error. We can identify those parts of a circuit that are contributing to the static short-circuit current at any instant. The ratio of the dynamic-short circuit charge $Q_{dsc}$ to the capacitive charge $Q_{cap}$ can be used to identify circuit parts that can be optimized. Figure 1 shows the variation of $Q_{dsc}/Q_{cap}$ with the load capacitance $C_L$ for different input slew $\delta$. This ratio increases with increasing input slew and decreasing load capacitance. A large value of this ratio indicates one of two possible situations. A very slow input or a very fast output generally leads to a large value of the ratio $Q_{dsc}/Q_{cap}$. When the ratio is more than 1, there is a clear opportunity to improve the circuit by either increasing the previous driver in order to reduce input slew, or by reducing the driver size if the load capacitance is small. The second alternative, if available, will not only reduce the power consumption of the load but will reduce the power consumption of the previous driver since it now drives a reduced load itself. Any stage in a circuit that has large values of $Q_{dsc}/Q_{cap}$ can be easily identified and reported for possible optimization.

The dynamic short-circuit ratio is not just a static property in a circuit. In multi-input gates, for example, NAND gates, different dynamic short-circuit ratios come into effect when all inputs are switching from low to high than when all but one input are high and only one input is switching from low to high. Current, charge and delays are significantly different in these two situations and can be estimated accurately using the dynamic short-circuit ratio.

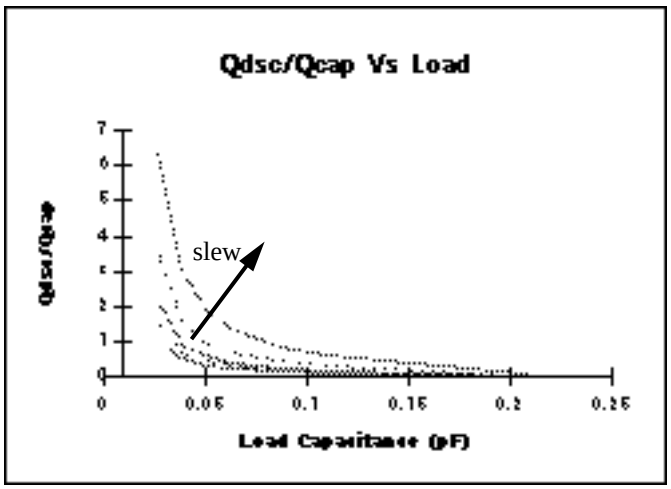


Figure 1: Ratio of dynamic short-circuit charge to capacitive charge as a function of load capacitance and input slew. For large slew and small capacitance the dynamic short-circuit charge exceeds the capacitive charge.

We describe in this paper a current analysis tool Lsim Power Analyst™ that operates at the switch-level abstraction. A one time (per technology) technology characterization step is performed in which delay, peak currents and charge per transition are measured while varying input slew, output load capacitance, driver size and dynamic short-circuit ratio.

## II Current and Charge Estimation

In general, total current drawn decreases with increasing input slew, and increases with increase in load capacitance and driver size. The dynamic short-circuit current, however, decreases with increasing slew up to moderate values of input slew and then starts increasing. From a low power circuit design perspective, the dynamic short-circuit current is a very good indicator of where a circuit stage is either over-loaded or under-driven.

We characterize the variation of current and charge with the dynamic short-circuit ratio using the inverter of Figure 2. Load capacitance and input slew were held constant while *wp / wn* was varied from 1:16 to 16:1. Figures 3 and 4 show the *Vdd* and *Vss* currents and charge associated with a low to high and high to low transition with varying dynamic short-circuit ratio. The currents and charge for a high to low transition are shown with the subscript *L* while those for a low to high transition are denoted by *H*. Note that the *Vdd* current and charge *iVddL, QVddL* and the *Vss* current and charge *iVssH, QVssH* represent the dynamic short-circuit current and charge for the high to low and low to high transitions respectively.

Consider the *Vdd* and *Vss* currents for a high to low transition denoted by the curves iVddL and iVssL. The *Vss* current iVssL increases as the *wp:wn* ratio goes from 1:1 to 1:16 mainly because of the increases in the size of the n-type transistor discharging the output. The dynamic short-circuit current iVddL shows a comparable increase. When *wp:wn* is varied from 1:1 to 16:1 the *Vss* current remains virtually constant while the dynamic short-circuit current iVddL increases quite rapidly. This clearly shows the dependency of the dynamic short-circuit current on the dynamic short-circuit ratio. As we pointed out in section 1, the ratio of the total current to the dynamic short-circuit current is a very good indicator of how wasteful a CMOS gate is in terms of power. From Figure 3, we can

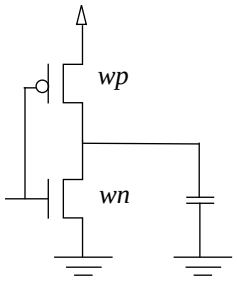


Figure 2: Inverter for characterizing charge and current.

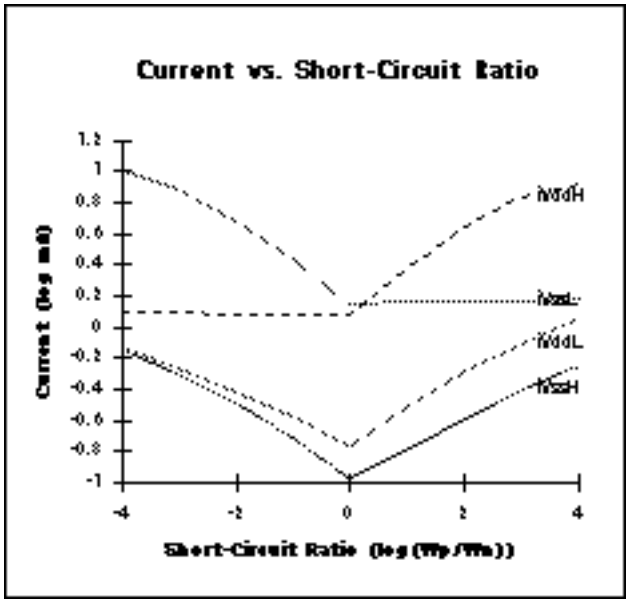


Figure 3: Peak current variation with dynamic short-circuit ratio.

observe that for a 16:1 ratio, the dynamic short circuit currents almost as large as the total of the dynamic short-circuit and capacitive current. The currents behave similarly for the low to high transition.

Figure 4 shows the variation of charge also illustrates the importance of the dynamic short-circuit ratio in determining the dynamic short-circuit charge and also the total charge. The plots for QVddL and QVssL for a ratio of 16:1 shows that the dynamic short-circuit charge QVddL is more than 50% of the total charge QVssL.

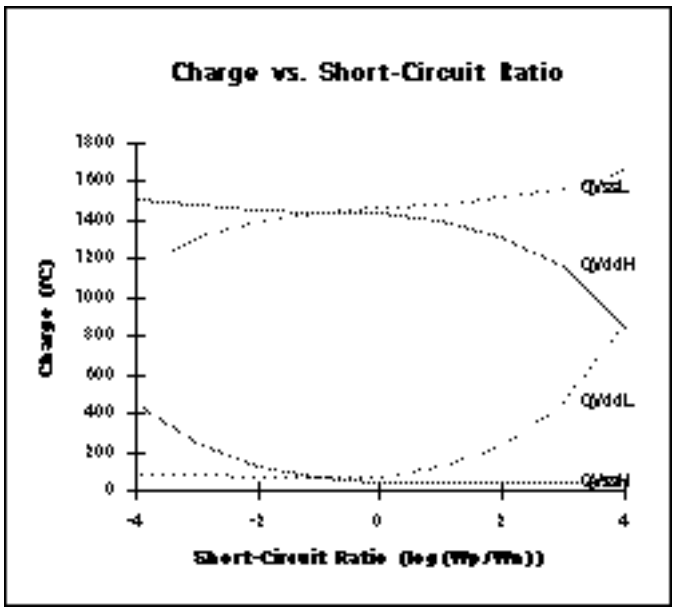


Figure 4: Total and short-circuit charge variation with short-circuit ratio.

### A Switch-level Algorithm

The current and charge analysis capability of Lsim Power Analyst is built on top of the switch-level timing simulation algorithm SPS (series-parallel switch) [4]. In a static compile step, the algorithm partitions the circuit into channel-connected components (*ccc*). A *ccc* consists of transistors that are connected via source-drain channels. Each *ccc* is then partitioned into biconnected components [5], thus forming a tree of bicomponents. Each bicomponent is then reduced via series-parallel reduction. *Driving-point resistances* [4] of each node to *Vdd* and *Vss* along with *Elmore delay* [6] can be computed. The algorithm takes advantage of the series-parallel and tree bicomponents by employing a linear time algorithm on these parts. Charge-sharing analysis is explicitly performed.

Once the switch-level algorithm has computed driving-point resistances, the new state of each node is computed and thus the nodes that are changing state are identified. For each ccc, one of three conditions are identified prior to performing current and charge estimation: *dynamic short-circuit*, *static short-circuit*, or *no short-circuit*. The no short-circuit situation involves transitions due to charge-sharing or transitions in which a node goes from a non-driven to a driven state. For each of these three conditions, the current and charge drawn from the Vdd and Vss nodes are estimated.

### B Dynamic Short-Circuit

A dynamic short-circuit situation exists when a path(s) to Vdd is turning off and a path(s) to Vss is turning on or vice versa. The dynamic short-circuit ratio $\boldsymbol{r_{dsc}}$ is determined by identifying in the algorithm the resistance of the path(s) that is turning off and the path(s) that is turning on. This is available after the driving-point resistances are computed. Note that traditional switch-level algorithms would find this to be a challenge since such algorithms cannot distinguish path(s) that are turning off. Also, the ability to accurately compute driving-point resistances is a requirement for correctly determining $\boldsymbol{r_{dsc}}$.

The load capacitance $C_L$ is determined from a knowledge of the nodes that are changing state. A ccc that has multiple nodes changing state has an effective load capacitance that is the sum of the capacitances of all nodes changing state.

### Input Slew Propagation

The input slew $\delta$ is required to estimate current and charge. When a single input is switching, the input slew is obviously that of the input that is switching. However, in a *ccc* with multiple inputs changing, or when some inputs have switched causing the transistors to be on, the selection of the appropriate input slew is not obvious. We compute the *effective input slew* by considering series-parallel components. This is illustrated in Figure 5. For series connected transistors, the effective input slew of a node is the maximum input slew of all the inputs that are switching in the series path. For parallel components, the effective input slew is the minimum input slew of each path in parallel. Inputs that are not switching are consid-

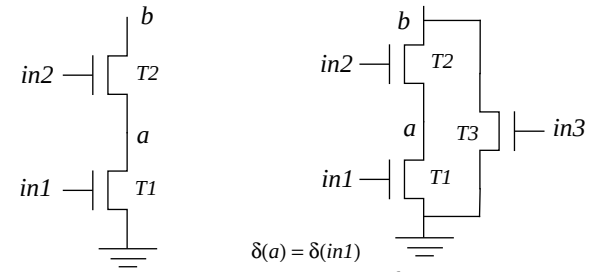


Figure 5: Propagation of input slew across series-parallel components.

ered to have zero input slew. We can apply this technique to not only series-parallel components, but also to those that are more densely connected.

This method works well for even complex series-parallel and other general structures. It is similar to that described in [7] recently for computing an effective input transition time. Once the effective input slew at a node is determined, the Vdd and Vss currents and charge can be obtained from the technology table for the particular short-circuit ratio and load capacitance. A knowledge of the transition (to high or low) then allows the algorithm to identify the total and the dynamic short-circuit current and charge and appropriately separate these two components.

Note that we do not estimate either current or charge indirectly. The direct look-up of current and charge for both the total and the short-circuit component is important in achieving high accuracy. In [2], the short-circuit current was computed from the charge and delay by dividing the charge by the delay; we believe that such indirect estimation inherently leads to inaccuracies as an inaccurate delay estimation will affect charge and current estimation.

### C Static Short-Circuit

The second situation that is identified for a ccc is a static short-circuit. This situation occurs when a node (or nodes) is driven to both *Vdd* and *Vss* simultaneously. For each such path between the *Vdd* and *Vss* nodes, the resistance of the path is used to look-up the static current from the technology table. By using a characterized I-V table, we are able to handle the non-linear nature of the transistor I-V characteristics properly.

The ability to explicitly obtain the static short-circuit current results in the capability to easily identify any such short-circuits in even large circuits. A designer could, for example, trace the static short-circuit current, stop the simulation when this current is non-zero and ask the tool to display all (or some) paths that are responsible for this current. Any design or timing error leading to such a situation can thus be very easily found and corrected.

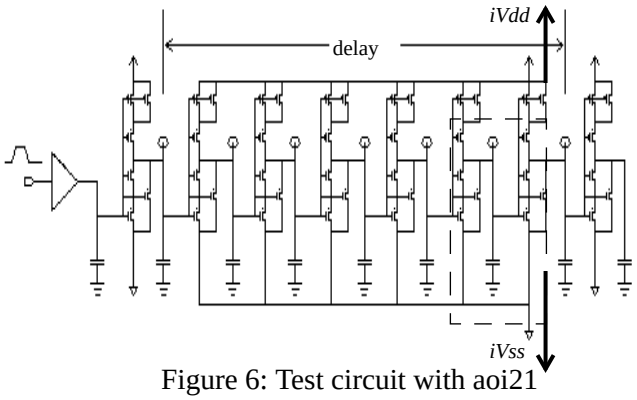


Figure 6: Test circuit with aoi21

### D No Short-Circuit

In this situation, node transitions are occurring due to charge-sharing or due to a transition from a non-driven state to a driven state. For transitions due to charge-sharing, we do not compute any currents making the implicit assumption that no current will be drawn from either *Vdd* or *Vss* nodes. For transitions from a non-driven to a driven state, we employ the same computation method as in the dynamic short-circuit case, but do not apply any of the dynamic short-circuit current and charge. This is because a transition that does not establish a dynamic short-circuit does not consume any dynamic short-circuit current or charge.

### E Results

We present results obtained from Lsim Power Analyst and compare it with that obtained from the circuit simulator Eldo®. Eldo is a high performance analog electrical circuit simulator similar to SPICE. The circuits that we used vary from simple inverters to nand and nor gates to and-or-invert gates. We used a chain of six stages of logic and measured current drawn by the chain as shown in Figure 6. Table 1 show the data. Per cent error from Eldo results are usually within 10%.

It is interesting to point out the three nand gate examples used in Table 1 denoted by the names *na2_1_2a*, *na2_1_2b* and *na2_1_2ab* and shown in Figure 7. These are three identical 2-input nand gates with a identical p-type transistors of size 1x and identical n-type transistors of size 2x. The three cases represent three different ways the inputs were excited. In

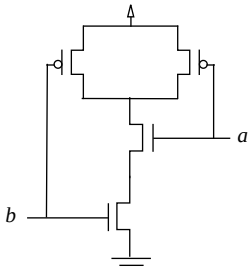


Figure 7: Nand gate example shown in Table 1.

Table 1: Comparison of average current obtained from Lsim Power Analyst and Eldo.

| Average Current (mA) | Eldo | | LPA | | % Error | |
|---|---|---|---|---|---|---|
| Circuit | iVdd | iVss | iVdd | iVss | iVdd | iVss |
| inv1_1 | 0.188 | 0.188 | 0.181 | 0.181 | -3.72 | -3.72 |
| inv4_2 | 0.309 | 0.309 | 0.280 | 0.285 | -9.39 | -7.77 |
| aoi21_2_2c50abc | 0.254 | 0.254 | 0.235 | 0.234 | -7.48 | -7.87 |
| na2_1_2a | 0.129 | 0.130 | 0.117 | 0.117 | -9.30 | -10.00 |
| na2_1_2b | 0.160 | 0.160 | 0.153 | 0.154 | -4.38 | -3.75 |
| na2_1_2ab | 0.129 | 0.129 | 0.120 | 0.121 | -6.98 | -6.20 |
| no2_2_1c50ab | 0.228 | 0.228 | 0.208 | 0.207 | -8.77 | -9.21 |
| no2_2_1b | 0.208 | 0.207 | 0.193 | 0.192 | -7.21 | -7.25 |

*na2_1_2a* and *na2_1_2b* only one input is changing, namely the input *a* and *b* respectively while the other input is permanently high. In *na2_1_2ab* both inputs are changing simultaneously. When both inputs change simultaneously, the nand gate behaves as a gate with a 2:1 pull-up to pull-down ratio; when only one input change it behaves as a 1:1 gate. The current in *na2_1_2b* is larger than in *na2_1_2a* by almost 20% due to the extra capacitance of the internal node that is discharged. One would expect a larger short-circuit average current (charge) in the gate with the 2:1 ratio. However, the gate *na2_1_2ab* has a faster rise time due to the two p-type transistors acting in parallel (refer to section 3.1) Therefore, the average currents for *na2_1_2a* and *na2_1_2ab* are similar because the reduced input slew for the rising input offsets the increased current due to the 2:1 ratio.

## III Delay Estimation

The primary goal of this work was to accurately estimate current and charge and to this end we introduced the dynamic short-circuit ratio as a modelling parameter. It turns out that this also results in significantly more accurate delay estimates.

Figure 8 shows the variation of delay with load capacitance and input slew and a fixed short-circuit ratio, again obtained from circuit simulation. The delay varies almost (but not exactly) linearly with load capacitance. This kind of relationship is typical of current sub-micron technologies. Figure 9 shows the variation of delay with the short-circuit ratio, where load capacitance and input slew have been kept constant. We notice that there is a non-negligible dependence of the delay on the short-circuit ratio. Based on these characteristics, we use the following delay model:

$$\Delta = R(r_{dsc}, \delta)\, C_L + \Delta_{nl}(r_{dsc}, \delta) \qquad (1)$$

A transistor is modelled as a resistive switch where the resistance $R$ is a function of the dynamic short-circuit ratio $r_{dsc}$ and the input slew $\delta$; we explicitly model a no load delay $\Delta_{nl}$ as given in (1), also as a function of $r_{dsc}$ and $\delta$. We contrast this to the usual way (2) delay has been modelled at the switch-level [8]. By using the model of (1) we gain significant accuracy. First, since the delay varies fairly linearly with load capacitance as depicted in Figure 8, we can obtain reasonable accuracy by keeping the resistance $R$ of a switch independent of the load capacitance while keeping the delay computation algorithm simple. The model of (2) forces the resistance $R$ be a highly non-linear function of the load capacitance and extremely sensitive to it, as depicted in [8]. This in turn leads to a large rippling effect; inaccuracy in estimating capacitance leading to inaccuracy in estimating $R$. Even more important is the way the delay scales with the size of the driver. We have found that only the *RC* delay scales linearly with size, but the no-load delay remains virtually constant as the driver size is changed. Thus, the model of (2) would cause the resistance $R$ to be a non-linear function of the transistor size also. Using our model avoids both these difficulties.

$$\Delta = R(\delta)\, C_L \qquad (2)$$

We gain accuracy in estimating delay by utilizing the dynamic short-circuit ratio. The resistance of a switch is obtained via table lookup using the dynamic short-circuit ratio $r_{dsc}$ and the input slew $\delta$. The dynamic short-circuit ratio $r_{dsc}$ is available after driving-point resistances have been computed. The input slew $\delta$ is obtained by propagating the input slew of gate nodes that are switching across series and parallel components as described in the previous section. Note here that the no-load delay is propagated similar to the input slew as depicted in Figure 5.

### F Results

We present a comparison of delay as estimated in Lsim Power Analyst and that obtained from Eldo for the same set of circuits as in section 3 in Table 2. As before, delay was measured across six stages of logic for both high and low going edges.

Delay estimates are typically within 10% of Eldo. We point to the three NAND gates *na2_1_2a*, *na2_1_2b* and *na2_1_2ab*. Note that the delay when only input *a* changes is significantly smaller (~ 20%) than when only input *b* changes. This is due

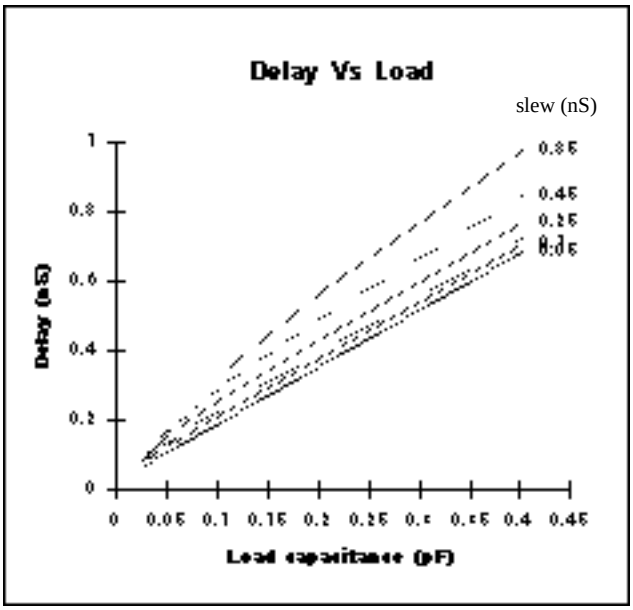


Figure 8: Delay variation with load capacitance and input slew.

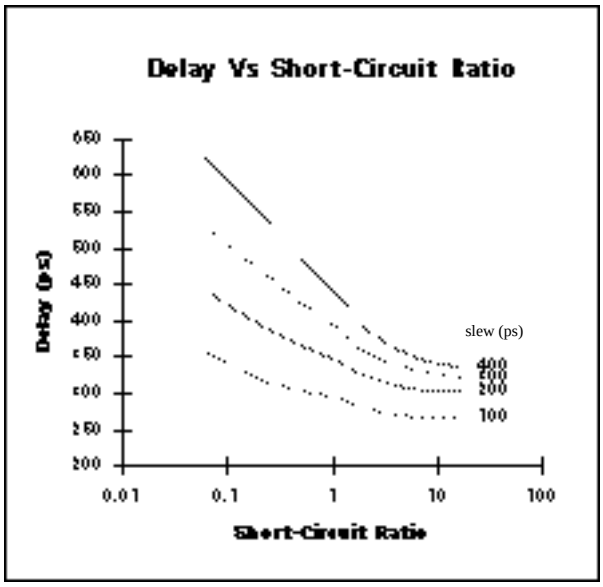


Figure 9: Variation of delay with short-circuit ratio for different input slew and fixed load capacitance.

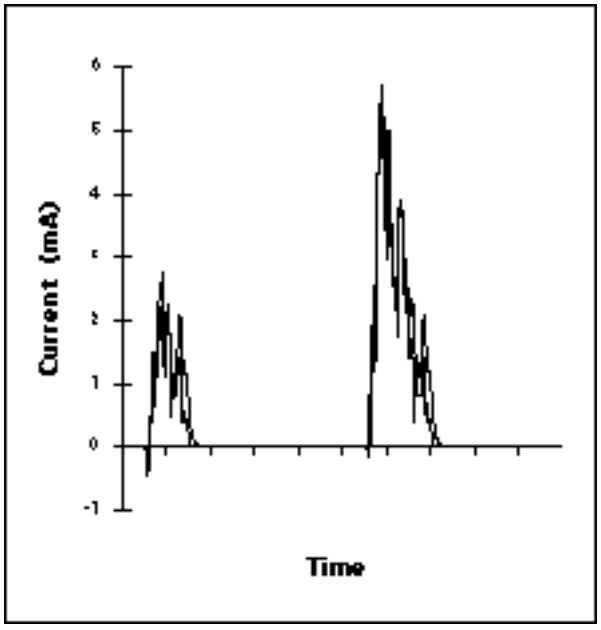


Figure 10: Instantaneous current waveforms from Lsim Power Analyst and Eldo for a 4-bit adder circuit.

to the extra capacitance of the internal node that needs to be driven when input *b* changes. When both inputs change simultaneously, the delay is almost 20% smaller than when only input *a* changes. This is principally due to the stronger pull-up of the two parallel p-type transistors. The case when both inputs are changing requires propagation of the no-load delay across the series transistors in the pull-down network. The accuracy of the results is a validation of the delay model, the use of the dynamic short-circuit ratio and the way the no-load delay is propagated across series parallel components. We point to the aoi circuit as an example where use is made of the dynamic short-circuit ratio as well as the no-load delay propagation across both series and parallel components.

## IV Conclusion

We have described techniques for estimating current, charge and delay in CMOS circuits at the switch-level abstraction. We use a one-time (per technology) calibration using a circuit-level simulator to build tables describing how these three quantities vary when four circuit parameters, namely, load capacitance, input slew, driver size and dynamic short-circuit ratio are varied. We specifically introduce the dynamic short-circuit ratio in order to accurately model current, charge and delay. We show that use of these four circuit parameters and appropriate selection of algorithms to use these parameters during simulation allows us to obtain results that are typically accurate to within 10% of circuit-level simulation. Figure 10 shows the instantaneous current plot for a four bit adder obtained from Eldo and Lsim Power Analyst. Performance of our algorithm is at least three orders of magnitude faster than a circuit-level simulator.

Table 2: Comparison of delay obtained from Lsim Power Analyst and Eldo.

| Circuit | ELDO (nS) | LPA (nS) | % Error |
|---|---|---|---|
| inv1_1 | 1.756 | 1.676 | -4.50 |
| inv4_2 | 0.984 | 0.939 | -4.52 |
| aoi21_2_2c50abc | 1.561 | 1.504 | -3.65 |
| na2_1_2a | 1.000 | 1.054 | 5.35 |
| na2_1_2b | 1.206 | 1.297 | 7.59 |
| na2_1_2ab | 0.768 | 0.819 | 6.64 |
| no2_2_1c50ab | 1.433 | 1.320 | -7.92 |
| no2_2_1b | 1.635 | 1.623 | -0.73 |

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