A New Built-In Self-Test Approach for Digital-to-Analog and Analog-to-Digital Converters

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Abstract

This paper proposes a test approach and circuitry suitable for built-in self-test (BIST) of digital-to-analog (D/A) and analog-to-digital (A/D) converters. Offset, gain, linearity and differential linearity errors are tested without using test equipment. The proposed BIST structure decreases the test cost and test time. The BIST circuitry has been designed to D/A and A/D converters using CMOS 1.2 µm technology. By only a minor modification the test structure would be able to localize the fail situation. The small value of area overhead (AOH), the simplicity and efficiency of the proposed BIST architecture seem to be promising for manufacturing.

Introduction

Effective methods for testing the digital circuitry are known, but testing the analog circuitry is still a problem. A great deal of effort has been devoted to testing pure analog circuits [3],[5]. Approaches for designing testable analog and mixed circuits have also been reported [6],[8], but up to now there is no general and efficient solution. The most frequently encountered parts of mixed digital and analog circuits are digital-to-analog (D/A) and analog-to-digital (A/D) converters, which bridge the gap between digital and analog systems. Many articles have been published about the design, specification and applications of D/A converters. Unfortunately, little has been written about testing conversion products [2] that need expensive mixed-signal test equipment. Appropriate BIST methods solve these problems, because test equipment is not needed.

The goal of this work is to propose an optimized BIST approach to automatically test the linearity and differential linearity errors, offset voltage (V_{OSE}) and gain error (G_{FSE}) of D/A converters. Then, the same BIST approach is mapped to A/D converter testing.

A BIST Scheme for D/A Converters

The area overhead (AOH) is one of the most essential problem of the analog BIST approaches. In order to reduce the AOH, the proposed BIST structure does not use a reference D/A converter that normally has 3 to 4 more bits of resolution, as presented in previous works [2],[4].

A. *BIST Architecture for D/A Converter Testing*

Fig. 1 illustrates the proposed approach for testing some static characteristics of a D/A converter in order to verify its functionality. When the Test input becomes active, the control logic (CL) begins the test procedure and directs the operation of the counter, D/A converter, analog switches and analog multiplexer (AMUX), and observes the output of the comparator.

This BIST structure tests V_{OSE}, differential linearity, $\varepsilon_{i,i-1}$, at all 2^N input codes, G_{FSE}, and linearity, ε_i, at 7 critical values. They are measured as follows:

$$V_{OSE} = V_O(00...0) - GND \quad (1)$$

$$G_{FSE} = V_O(11...1) + 1\ LSB - V_{REF} \quad (2)$$

$$\varepsilon_{i,i-1} = V_O(i) - V_O(i-1) - 1\ LSB \quad (3)$$

$$\varepsilon_i = V_O(i) - (b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) \times V_{REF} \quad (4)$$

where $i = (b_1 b_2 b_3 ... b_N)$

The measured parameters are alternately compared with values 1/2 LSB and -1/2 LSB (or maximum acceptable tolerance margin) to verify whether or not they are smaller than the maximum allowance error voltage.

B. *Autozeroing Technique*

During autozero cycle (AZC), AZ is active and AMUX selects GND. Thus, operational amplifier (OA) is connected in the unity gain configuration and the input offset is available at the output. Capacitor C_{AZ} stores the offset across its terminals. After applying the offset-cancellation algorithm, C_{AZ} is placed in series with V_{OS} at the noninverting input of the OA to cancel the existing offset voltage. The idea of offset-cancellation offers the possibility of automatically nulling the offset voltage without using external pins.

C. *Test procedure*

When the Test input becomes active, the control logic performs a self testing to verify the functionality of the test circuitry. Then, it begins the D/A converter testing. The test algorithm consists of the following phases:

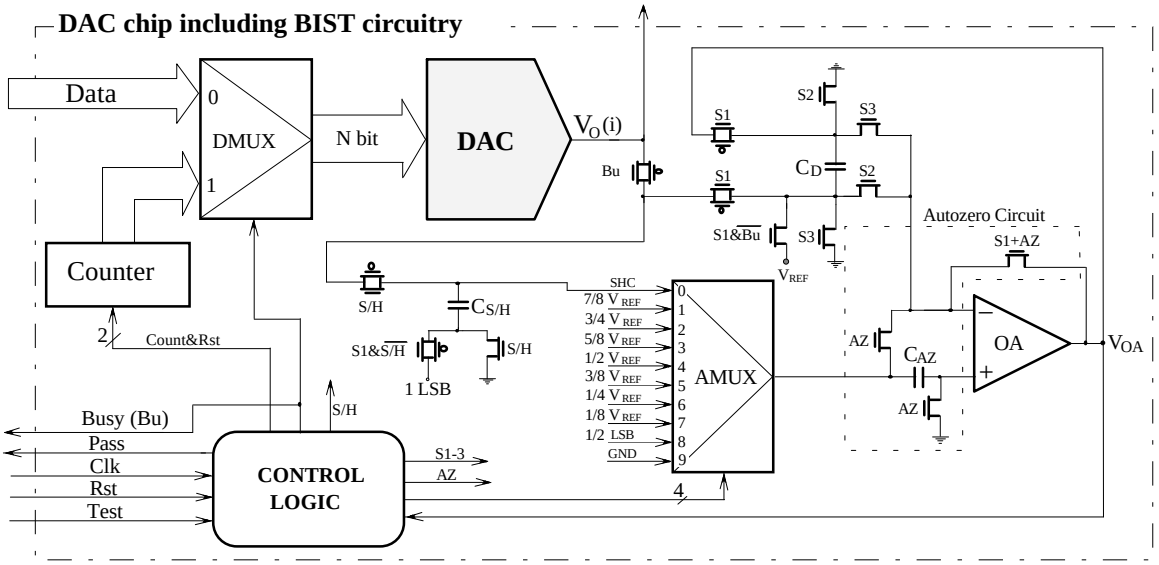

Fig. 1. The architecture of the fast BIST approach for D/A converter testing.

Self-testing:

At the first self-test cycle, the S1, S/H and AZ signals are active and Busy is inactive, thus $C_{S/H}$ is charged to V_{REF}. At the second self-test cycle, Busy remains inactive, AMUX selects SHC and S1 becomes active, thus C_D is charged ideally to 1 LSB. Then, AMUX selects ½ LSB, the S3 and S2 become alternately active resulting in the comparison between the C_D voltage and ±½ LSB. The output of the OA is verified by the CL and must be 1 and 0 consequently. In this way, the functionality of the test structure, except for the counter and digital multiplexer (DMUX), is verified. The counter and the CL could be tested by a scan-based BIST technique. The self-test phase takes 4 clock cycles.

V_{OSE} testing:

Counter=0, the autozero cycle is performed. At the second cycle, AMUX selects GND and S1 becomes active therefore capacitor C_D is charged to the V_{OSE} (AZ=0). At the last two cycles of V_{OSE} testing, AMUX selects ½ LSB and S3 and S2 become active consequently resulting the V_{OSE} to be compared with ±½ LSB. In both cycles, the V_{OA} is verified by CL. This phase takes 4 clock cycles.

***Differential linearity error (DLE), $\varepsilon_{i,i-1}$, testing*:**

During DLE testing the following operations are performed: V_O is held in the $C_{S/H}$ by activating S/H signal (1st cycle). The AZC is executed and the counter is incremented (2nd cycle). Then, AMUX selects the output of SHC and S1 becomes active (3rd cycle). Therefore, the capacitor C_D is charged to the $\varepsilon_{i,i-1}$. At last two cycles, AMUX selects ½ LSB and S3 and S2 become active consequently. In both cycles, the V_{OA} is verified by CL, therefore V_{OSE} is compared with ±½ LSB. The DLE testing procedure takes 5 clock cycles for each input code, therefore the total DLE testing time is:

$$T_{DLE}=5\times 2^N/f \qquad (5)$$

where f is the clock frequency of the test circuitry.

Linearity error (LE), ε_i, testing:

Counter=($b_1b_2b_300...0$), AZC is performed and then AMUX selects $(b_12^{-1}+b_22^{-2}+b_32^{-3})\times V_{REF}$ and S1 becomes active. Therefore, C_D is charged to ε_i. At the last two cycles, the ε_i is compared with ±½ LSB. In this phase, the deviation of the output voltage of the D/A converter from the ideal values corresponding to the three most significant bits is tested. The LE testing phase takes 4 clock cycles, therefore complete LE testing takes 28 clock cycles.

***G_{FSE} testing*:**

Counter=(11...1), AZC is accomplished and $V_O(i)$ is held in $C_{S/H}$ by activating S/H signal. Then, Busy signal becomes inactive, AMUX selects SHC, and S1 becomes active. Thus, C_D is charged to the G_{FSE}. Finally, G_{FSE} is compared with ±½ LSB at the last two cycles. G_{FSE} testing phase takes 4 clock cycles.

As explained above, after each phase of test, the measured parameters are alternately compared with +½ LSB and -½ LSB by means of the OA that has ½ LSB at its noninverting input and the C_D voltage or the inverse of C_D voltage at its inverting input. The output of the OA represents the result of test and is evaluated by the CL. This structure exercises all 2^N codes measuring and evaluating V_{OSE}, G_{FSE}, $\varepsilon_{i,i-1}$, and ε_i (for the last three significant bits) in total time:

$$T_{TOTAL} = (40+5\times2^{N})/f \quad (6)$$

where f is limited by the combined settling time of the D/A converter and the OA. We can assume that the total test time is approximately equal to T_{DLE}.

A BIST Approach for A/D Converters

A/D converters can be classified under three categories: 1) The A/D converters using D/A converters, 2) The integrating types A/D converters, and 3) The flash A/D converters.

The first category is often preferred as the majority of the additional circuitry are digital and therefore easily implemented in CMOS technology. This kind of converter includes the successive approximation-type converter and thestaircase-type converter which employ a D/A converter, a counter and a comparator in a feedback loop with control logic. Fig. 2 shows the block diagrams of a successive approximation A/D converters.

Each digital output code corresponds to a continuous range of analog input values. Hence, the functional testing of A/D converters is more complex than D/A converters and therelated BIST architecture results in a higher AOH. In this section, we propose a technique for testing of A/D converters based on the BIST technique developed for D/A converter testing in previous sections.

The main idea is to reconfigurate the A/D converter architecture in the test mode and then to test its internal D/A converter. In this way, the functionality of the internal blocks of the A/D converter is verified, because all of them contribute in the D/A converter testing.

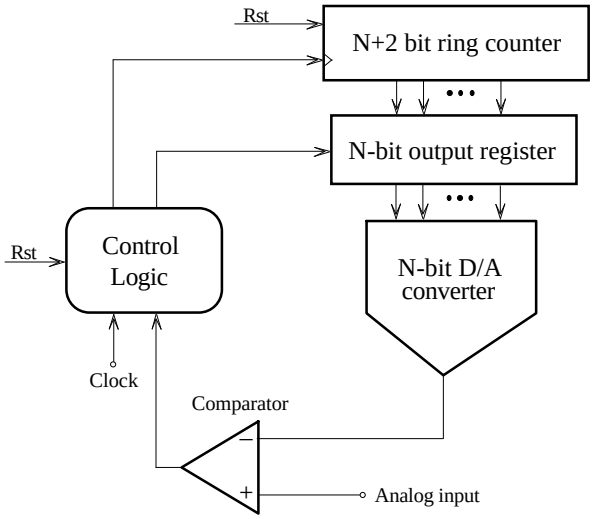

Fig. 2. Successive approximation D/A converter.

Fig. 3 shows a BIST architecture for the successive approximation A/D converter. In the conversion mode, the AMUX selects Analog input (10) and Bu and other control signals are set to 0. Therefore, the test circuitry is disabled and D/A converts the input analog voltage. This approach has the following advantages:

1) Its AOH is very small, because the BIST architecture utilizes the comparator and the counter that are already available in the A/D converter. The AOH is related to analog switches, voltage references and a portion of control logic that occupy a very small chip area. Therefore, the required BIST circuitry for A/D converter is much smaller than that for D/A converter. In general, the AOH related to this technique amounts less than 5% of the total active chip area.
2) Direct functional testing an A/D converter is a time-consuming process, because the input voltage must be slowly varied to find the transition voltages. The known methods to speed up the process of finding transition voltages, such as a computer-controlled D/A converter or a servo loop to automatically adjust

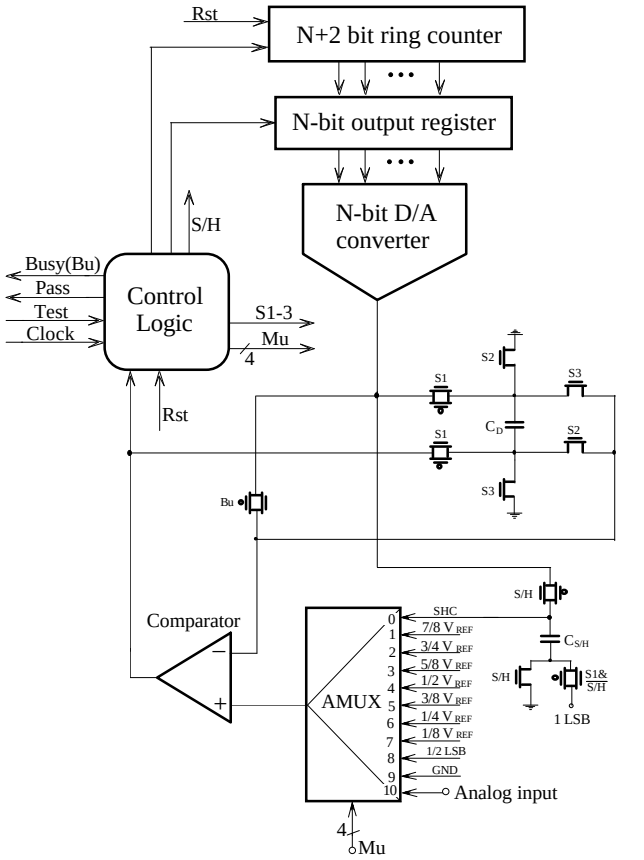

Fig. 3. The BIST architecture for successive approximation A/D converter.

the input voltage,are not appropriate for BIST approach. The same test procedure is performed for both D/A and A/D testing. Therefore, the D/A and A/D test time by the BIST presented in this paper are similar.

3) The possibility of testing the internal D/A is advantageous, because the precision of the A/D converter depends directly on the precision of its D/A converter. If the D/A converter that is used in an A/D converter is nonlinear, the step size will deviate from the ideal 1 LSB step size [4].
4) The proposed BIST structure is very easy to realize, because it does not need the additional high quality blocks. Furthermore, it does not use the external test equipment during test phase.

As a result, this method reduces the manufacturing cost. The same approach can be applied to test all A/D converters employing D/A converter.

The integrating types and flash A/D converters can be tested by the reported approaches [2],[5],[7]. Unfortunately, these techniques are not suitable for BIST approach for A/D converter.

The flash A/D converter can be tested using a simple BIST approach. It comprises a voltage references bloc, a large number of comparators and a digital decoding network. Hence, a BIST circuitry may be incorporated for comparator testing. The implemented BIST circuitry selects one of the comparators each time and applies a given test signal to it. The selecting and evaluating procedure can be managed by a CL. The digital section of the A/D converter may be evaluated by a Scan-BIST technique.

BIST Results

By eliminating the test equipment. the total test time by the BIST has been reduced to approximately $5\times2^N/f$ s for A/D and D/A converter testing. Because, the time needed to calibrate external equipment and calculate the parameters by a processor is saved.

The circuit was designed using CMOS 1.2 μm technology. The proposed test structure was simulated and evaluated for a 12-bit D/A converter by exercising all 2^N input codes. The introduced V_{OSE}, DLE, LE and gain error (G_{FSE}) were fully detected by implemented BIST.

The simulations performed show that the switching circuit ensures the required accuracy for our application. The symmetry of switching process in the measurement part of the BIST architecture minimizes the error voltage that is introduced by parasitic capacitors.

These evaluations show that the BIST gives the same testability as conventional testing and is applicable to pass/fail D/A and A/D converters testing for manufacturing. The AOH related to the BIST structures based on the average area of medium to high-resolution D/A converters [1][7], amounts to less than 10% of the total active chip area and it will be still smaller for A/D converters.

Conclusion

A practical BIST approach for the functional testing of D/A converters has been presented and evaluated. An extension to A/D converter testing by applying the same BIST structure is also proposed. The BIST performs a self-test to verify its functionality and then begins D/A converter testing. The proposed BIST structure reduces the test time and the test cost. The obtained AOH is small and reasonable for mixed-circuit testing. Also, the proposed architecture is relatively simple. These results show that the proposed BIST design is applicable to the pass/fail testing of D/A and A/D converters and seems to be promising for manufacturing. With a minor modification, the test structure would be able to test all D/A converters on the chip that use the same reference voltage and have the same resolution. It would be also interesting to explore the testability of our approach to other mixed-circuit structures.

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