Unified Complete MOSFET Model for Analysis of Digital and Analog Circuits

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Abstract

In this paper, we describe the complete MOSFET model developed for circuit simulation. The model describes all transistor characteristics as functions of surface potentials, which are calculated iteratively at each applied voltage under the charge-sheet approximation. The key idea of this development is to put as much physics as possible into the equations describing the surface potentials. Since the model includes both the drift and the diffusion contributions, a single equation is valid from the subthreshold to the saturation regions. The unified treatment of our model allows all transistor characteristics to be calculated without any nonphysical fitting parameters. Additionally the calculation time is drastically reduced in comparison with a conventional piece-wise model.

1 Introduction

Till now it is believed that physically based implicit model including iteration procedures is computationally expensive and hence is not suitable for circuit simulation. Therefore, most of models are in closed form, describing transistor characteristics with analytical equations using radical simplifications [1]. These are the drift approximation, the channel length modulation, and the charge sharing approximation to include the short-channel effects. Other approaches are even though based on surface potentials as basic functions, either not all of the small geometry effects are included or some simplifying assumptions are made to save CPU time [2]. This results in loss of consistency, and thus no clear advantage could be demonstrated.

Pao and Sah have shown that the inclusion of the diffusion contribution together with the drift one results in smooth transitions among operating modes with a single equation [3]. It has been shown that the current equation is written analytically as a function of surface potentials only at the source side ϕ_{S0} and the drain side ϕ_{SL} under the charge-sheet approximation [4]. We have developed the model further to complete equations for circuit simulation by including the short-channel effect explicitly. The model was implemented into our standard circuit simulator TITAN. Our results show that correct development and treatment of the drift-diffusion approximation bring on a big advantage in circuit simulation, even if iterative procedures to calculate ϕ_{S0} and ϕ_{SL} are included.

2 Model Description

Our new MOSFET model is based on the charges controlled by voltages [5]. The basic equations for the inversion layer charge Q_i and the depletion layer charge Q_b are written at position y along the channel with the effective gate voltage V'_G

$$Q_i(y) = -C_{ox}(V'_G - \phi_S(y)) - Q_b(y) \tag{1}$$

$$Q_b(y) = -qN_{sub}L_D\sqrt{2\beta(\phi_S(y) - V_{bs}) - 1} \tag{2}$$

where q, C_{ox}, N_{sub}, L_D, and ϕ_S are the electronic charge, the oxide capacitance, the substrate doping concentration, the Debye length, and the surface potential at position y, respectively. The bulk voltage is denoted by V_{bs}, and the thermal voltage by β. Owing to the charge neutrality the gate charge Q_g is the negative sum of Q_i and Q_b.

The inclusion of the short-channel effect is done by introducing the lateral electric field E_y as [6]

$$V'_G = V_{gs} + \Delta V'_G - V_{fb} \tag{3}$$

$$\Delta V'_G = \frac{\epsilon_{si}}{C_{ox}}\sqrt{\frac{2\epsilon_{si}}{qN_{sub}}(\phi_S(y) - V_{bs})}E_{yy} \tag{4}$$

$$E_{yy} = \frac{dE_y}{dy} \tag{5}$$

which is the result of integrating the charge under the Gauss law at the gate voltage V_{gs} with the flat-band voltage V_{fb}. The gradient of the lateral electric field E_{yy} is extracted from measured threshold voltage V_{th}. At threshold $\Delta V'_G$ is represented by ΔV_{th}, which is the threshold voltage V_{th} reduction of the short-channel transistor from the long-channel one.

For circuit simulation all charge values on each node should be known. Therefore integrations of charges along the channel are necessary. The resulting charges Q_I, Q_B, and Q_G are independent of position [1]. The integration by position y is rewritten by potential $\phi_S(y)$, which results in final analytical equations being functions of the surface potentials ϕ_{S0} and ϕ_{SL}, only. The integrations and the derivatives of all equations required for circuit simulation can be expressed analytically in a straightforward but lengthy way.

The surface potentials are calculated iteratively. The potential ϕ_{S0} is calculated by solving the Poisson equation. For ϕ_{SL} the drift-diffusion approximation is solved iteratively in a form

$$\beta\phi_{SL} = \beta\phi_{S0} + \beta V_{ds} + ln\frac{Qi(L)}{Qi(0)} \tag{6}$$

under the assumption that the Fermi potential difference between the source side and the drain side is equal to the drain voltage V_{ds}.

The only fitting parameters which cannot be known from process flow, are those related to the mobility. These values are fitted to measured or numerically simulated $I-V$ characteristics, or are taken from standard values [7].

3 Computational Aspects

It is a prerequisite for the model to be used in standard circuit simulation, that the surface potentials ϕ_{S0} and ϕ_{SL} are computed very efficiently for every set of applied voltages.

As the Poisson equation and Eq. 6 are implicit, approximations or iterative methods are necessary. The difficulty here is that the accuracy requirements may become very severe in certain situations, as was pointed out by Turchetti and Masetti [8]. This was the reason for us to apply a classical Newton method, although in literature a variety of alternative approaches has been reported [4,9]. Our implementation is carefully damped mainly for preventing program aborts (e.g. due to negative arguments of square root) and for improving convergence. For numerical reasons Eq. 6 is rewritten in exponential form. Special care is taken to avoid numerical cancellation, which can be achieved by rearranging parts of the equations. As initial guess for Newton's procedure we use values based on simplified analytical solutions, or - at least in time domain analysis, where the voltage changes for subsequent calls of the model routine tend to be small - the solution of previous iterations. The convergence criteria are defaulted to 10^{-12} for the surface potentials and $10^{-7} * C_{OX}$ for the defect of the Poisson equation, which proved to yield sufficiently accurate and smooth transistor characteristics and derivatives. The number of iterations required to obtain convergence is typically between 1 and 7; further improvements are possible. The average number of iterations for a real application within the circuit simulation is typically between 2 and 3 (see Table 1), which is quite satisfactory. Until now we have not observed a failure of convergence (i.e. more than 20 iterations).

Table 1: Run Statistics for Different Examples

circuit	inverter chain	freq. divider (2 stages)	freq. divider (64 stages)
# of transistors	16	36	194
model	new/convent.	new/convent.	new/convent.
# of timepoints	441/456	1179/1198	22822/23385
# of iterations (circuit equations)	854/896	2050/2031	62955/63607
average # of iterations for ϕ_{S0}	3.0/-	2.8/-	2.8/-
average # of iterations for ϕ_{SL}	2.2/-	2.1/-	2.0/-
CPU time for model evaluation (sec)	6/9	30/48	4269/6806
CPU time total transient analysis (sec)	7/11	38/56	4600/7160

4 Results

Instead of real transistor and its measurements, first, we used simulated results with the mixed mode device/circuit simulator MEDUSA, which treats MOSFETs in full 2 dimensions [10].

Comparisons of DC results with those of MEDUSA are shown in Figs. 1 and 2 for the $L_{poly} = 0.2\mu m$ case at $V_{bs} = 0$. Due to the consistent description of our model, only 11 fitting parameters, including the temperature variation and the V_{bs} dependence, are sufficient for all channel lengths.

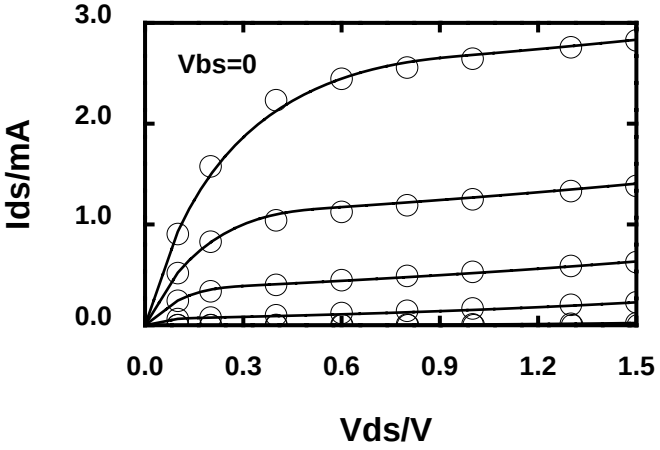

Figure 1: Comparison of I-V characteristics for $L_{poly} = 0.2\mu m$. Solid lines are with our model and open circles are results with MEDUSA.

Figure 3 shows calculated intrinsic capacitances as a function of V_{gs} for $L_{poly} = 10\mu m$. Due to both the drift and the diffusion contributions smooth transitions from the subthreshold region to the linear, and further to the saturation region are realized. These smooth transitions with a single equation are not only important for physical reasons, but also to keep consistency within the model. This consistency is important to reduce calculation time in circuit simulation. Table 1 shows some run statistics on test circuits for our model in comparison with a conventional model similar to BSIM2 for several examples. All computations were done on an HP9000 Series 750 workstation. The time for model evaluation includes the model frame, i.e. overlap capacitances, substrate diodes and so on, which is identical for both models.

Our new model includes two iteration procedures, one for ϕ_{S0} and for ϕ_{SL}. Although accuracy requirements are severe, the average number of iterations per model call is moderate. The number of iterations for solving the circuit equations, as well as the number

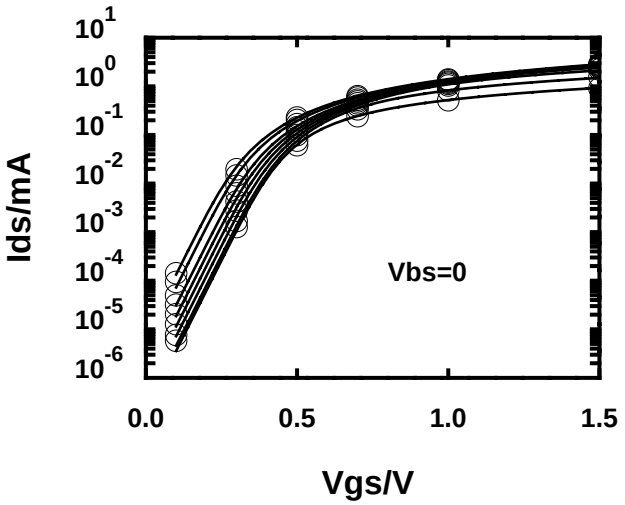

Figure 2: Comparison of I-V characteristics for $L_{poly} = 0.2\mu m$.

of timesteps are not much different from those for the conventional model.

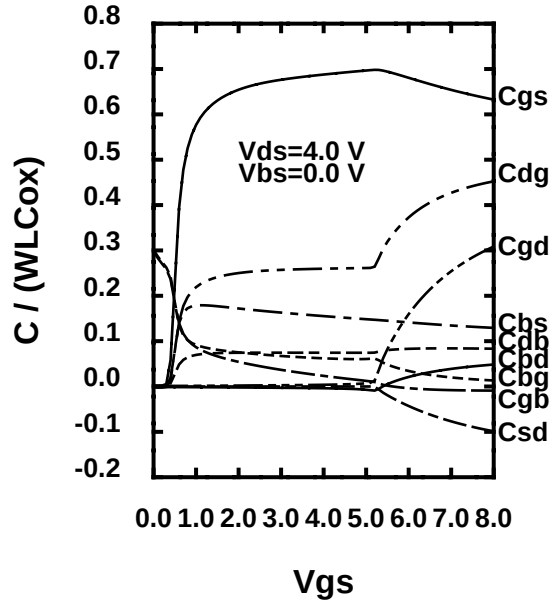

Figure 3: Calculated 9 independent intrinsic capacitances with our model for $L_{poly} = 10\mu m$ as a function of V_{gs}.

This is contrary to the Park et al. observation [2]. The reason is that the conventional model used for our comparison had smooth transitions between different modes of operation. The resulting CPU time reduction of our new model is remarkable even for small circuits. Park et al. have tried to reduce the CPU time by approximating functions for ϕ_{S0} and ϕ_{SL}, eliminating iteration procedures [2]. However, the price to be paid for this approach is loss of consistency, and additional expense for the evaluation of nonphysical, more complex equations and fitting functions. So their model tends to be more expensive than a conventional one.

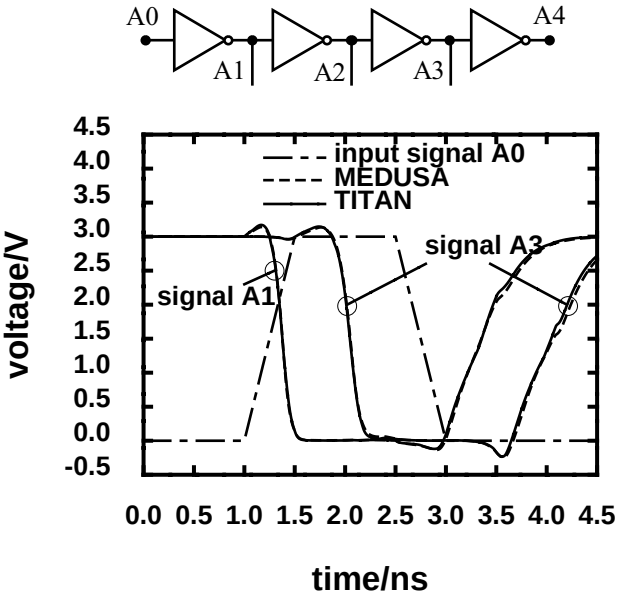

Figure 4: Comparison of an inverter chain response calculated with our model implemented into the circuit simulator TITAN and MEDUSA. The poly-gate lengths are 0.6 μm for n-channel and 0.7 μm for p-channel transistors. The channel width is equal to 20 μm.

Figure 4 shows the response of a CMOS inverter chain simulated with our new model comparing with MEDUSA results. Our model reproduces the MEDUSA result, not only the delay but also the total waveform, without any fitting parameters even in parasitic capacitances.

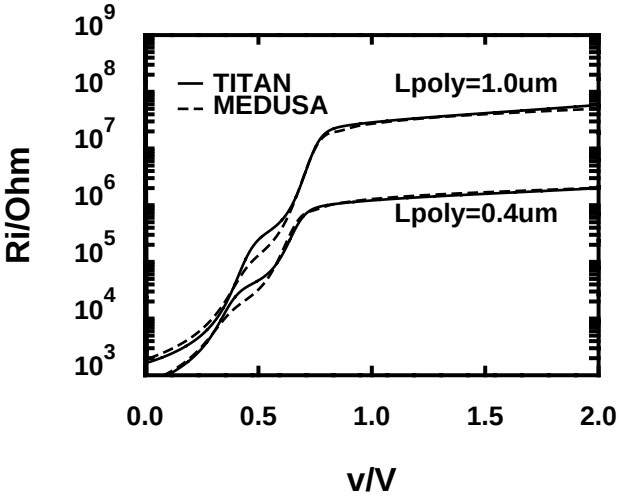

Figure 5: Comparison of a cascode output resistance calculated with our model in TITAN and MEDUSA.

Figure 5 shows a cascode (cf. Fig. 6) output resis-

tance R_i ($= \Delta v/\Delta i$) for two different channel lengths. Our model describes perfectly the saturation behavior, which is relevant for analog applications. Due to the increase of the high field effect, the gradient of the saturation region is supressed for reduced channel length. The deviation of our model from MEDUSA around $0.5V$ is due to the charge-sheet approximation, which will be improved in the near future.

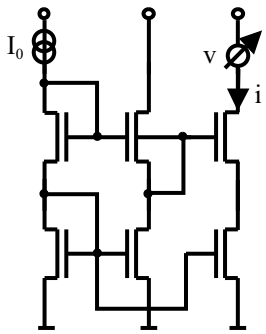

Figure 6: Schematic of a cascode used for Fig. 5.

A 23 stage ring oscillator is studied to verify our model for real applications. The calculated frequency was compared with measurements and also with results using the conventional model. Figure 7 shows relative errors of simulated results from measurements for different channel lengths at $V_{bs} = 0$. The measurements show larger deviation among different chips for shorter channel length and smaller power supply voltage V_{dd}. The deviations of the long channel (cf. the arrow a) and the short channel (cf. the arrow b) cases are depicted in the figure. Even though we have not introduced any fitting parameters to our calculations, the error is within the measurement deviation. On the contrary, the conventional model shows the clear applied voltage dependent deviation from the measurements, although it has approximately three times more fitting parameters than our model. This is due to the inaccurate physics behind the model description.

5 Conclusion

Our newly developed MOSFET model describes the whole range of applied voltages with a single equation due to the drift-diffusion approximation. All equations needed for circuit simulation are functions of the surface potentials, which are calculated iteratively. A single parameter set with a few fitting parameters is sufficient for a geometry range from long-channel transistors to channel lengths down to $0.2\mu m$ due to the consistent incorporation of the short-channel effect. We have shown here that our newly developed precise MOSFET model, though including iteration procedures, leads to significant reduction of calculation time, which is mainly due to its consistency and fast convergence of the internal iteration loops. This revolutionary fact allows us to use such precise MOSFET model in standard circuit simulation, which was previously considered to be impractical.

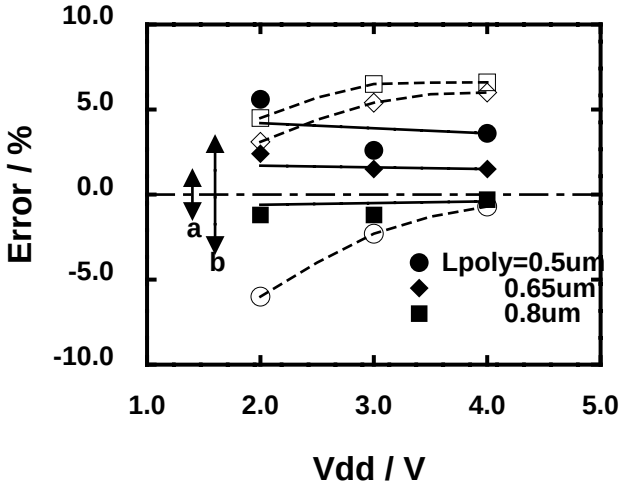

Figure 7: Relative deviation of calculated frequency results from measurements for a 23 stage ring oscillator. Solid lines are with our model and broken lines are with a conventional model similar to BSIM2.

6 References

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