Fast Transient Power and Noise Estimation for VLSI Circuits

Wolfgang T. Eisenmann
Motorola GmbH Munich
ASIC Design Automation
D-81829 Munich, Germany

Helmut E. Graeb
Technical University of Munich
Institute of Electronic Design Automation
D-80290 Munich, Germany

Abstract - *Today's digital design systems are running out of steam, when it comes to meeting the challenges presented by simultaneous switching, power consumption and reliability constraints emerging in VLSI circuits. In this paper a new technique to accurately estimate the transient behavior of large CMOS cell-based circuits in a reasonable amount of time is presented. Gate-level simulation and a consistent modeling methodology are employed to compute the time-domain waveforms for signal voltages, supply currents, power consumption and ΔI noise on power lines. This can be done for circuit blocks and complete designs by our new tool POWTIM, which adds SPICE-like capabilities to digital design systems.*

1 Introduction

The fast evolution of CMOS technology provides the increasing density and speed required to realize ever more complex designs running at ever higher frequencies. A set of tools has been developed to help the designer synthesize, simulate, layout and verify a circuit in terms of functionality and timing. In addition to these tasks, new problems have emerged as a result of higher currents and current densities. Power consumption, ΔI noise, hot electrons and electromigration can degrade the reliability of a design drastically and hence have become a major concern.

A number of approaches use SPICE to characterize average, RMS or maximum currents for a CMOS inverter. All other gates are transformed to an equivalent inverter. The total current is derived by summing up the individual currents under simultaneous and non-simultaneous switching conditions (as in [1]) or depending on input transitions ([2] and [3]). In [4] the signal waveforms are calculated using a switch-level timing simulator. There the capacitive and short circuit currents are approximated with a triangular model. Piecewise linear functions are employed in [5], and [6] uses exponential dependencies. In [2], [3], [5] and [7] the model of Fig. 1 is used for a generic CMOS gate. Eqn. (1) shows the supply current for a falling (rising) output transition assuming that no current

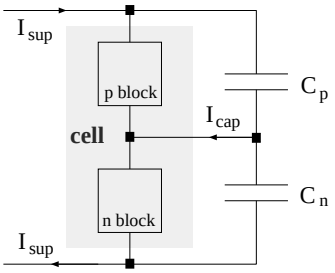

Figure 1: Widely used model for a CMOS cell

is flowing through the p-block (n-block). The short-circuit current and the input currents are neglected in the cell-model and during the derivation of eqn. (1).

$$I_{sup} = \frac{C_{p,n}}{C_p + C_n} \cdot I_{cap} \qquad (1)$$

Often the power is calculated from the derived supply current via multiplication with the constant supply voltage V_{DD}. Power is only dissipated in resistances (of transistors), hence the power must be calculated multiplying the drain-source currents with the time dependent drain-source voltages. Another shortcoming of previously reported methods is due to the chosen waveform models. To be consistent with formula (2), showing the noise n_X induced in an inductor L by a capacitive current i_X, a triangular current model can not be used together with a ramp function for the signal voltage v_X. Only a quadratic approach is electrically correct and leads to a rectangular noise model.

$$n_X(t) = L \cdot \frac{di_X(t)}{dt} = L \cdot C \cdot \frac{d^2 v_X(t)}{dt^2} \qquad (2)$$

This paper is organized as follows. A new and more general cell model that is applicable to complex library cells is introduced in Section 2. In Section 3 consistent waveform models are developed and discussed. Section 4 will give a brief overview about the tools we have created for automatic cell characterization, transient waveform estimation and average power calculation. In Section 5 the accuracy of the models will be shown, comparing the waveforms to SPICE results. Several hundred cells of a commercial ASIC library (Motorola's $H4C^{TM}$ submicron CMOS

technology [8]) have been characterized and are used in Section 6 to calculate the transient waveforms and the average power for benchmark circuits and industrial VLSI designs.

2 Cell-Based Modeling

In an ASIC environment, gate level logic simulation is used to verify a circuit in terms of functionality and timing. For timing characterization the cells are treated as black boxes, hence we try to do the same for power characterization. Figure 2 shows a black box cell and its terminal currents. Note that the cell is attached to different power/ground nodes than the output load. In physical design this is true since driver and receivers are placed at different locations on or off the chip. The new model can be reduced to the one shown in Figure 1 if the input currents are set to zero and the external supplies are tied to the cell supply nodes. Therefore the model in Figure 2 is a more general cell representation. According to Kirchhoff's law, the terminal currents are expressed in (3), where C_{X_j} is the load on output X_j and C_{A_i} is the cell-internal capacitance on input A_i.

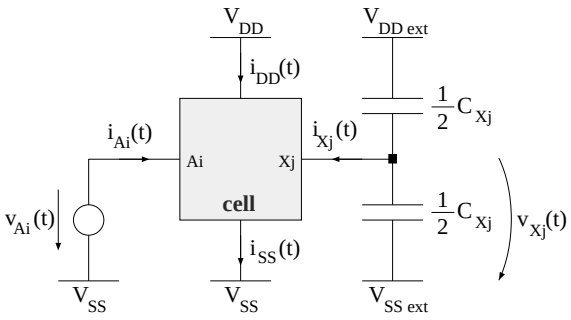

Figure 2: Black-box cell

$$i_{SS}(t) = i_{DD}(t) + \sum_j i_{X_j}(t) + \sum_i i_{A_i}(t) \qquad (3)$$

$$i_{X_j}(t) = -C_{X_j}\frac{d\,v_{X_j}(t)}{dt} \qquad i_{A_i}(t) = C_{A_i}\frac{dv_{A_i}(t)}{dt}$$

In order to save memory and CPU time, only the toggles on the outputs of a cell will be monitored during simulation. Therefore we don't know which one of the inputs caused the output to change its state. As a worst-case approximation it is assumed that always the longest path is active. This path is determined based on information available after timing characterization of a cell. Equations (4) and (5) describe the time dependent supply currents and power consumption of a path from input A to output X of a cell. Also the average power is given in equation (6) for an optional observation time T. During T any number of signal transitions N on X may occur, where $f = N/T$ is the toggle frequency and T_S is the time period used to average $i_{DD,SS}$ and i_A during characterization.

$$i_{SS}(t) = i_X(t) + i_{DD}(t) + i_A(t) \qquad (4)$$

$$p(t) = i_X(t)\,v_X(t) + (i_{DD}(t) + \frac{i_A(t)}{2})\,V_{DD} \qquad (5)$$

$$\overline{P} = \frac{1}{2}C_X V_{DD}^2 f + (\overline{I_{DD}} + \frac{\overline{I_A}}{2})\,T_S V_{DD} f \qquad (6)$$

If the power and ground networks are collapsed to ideal nodes supplied by only one package pin respectively, one simply has to add the currents and the power of all cells to get the overall chip supply currents and power consumption for a design. The noise induced in the package pin inductances by the supply currents is then expressed in (7).

$$n_{DD,SS}(t) = L \cdot \frac{d\,i_{DD,SS}(t)}{dt} \qquad (7)$$

3 Waveform Characterization

The supply currents in equations (4) and (5) are characterized using their highest values obtained from transistor level simulation ($i_{SS_{max}}$ for a rising output, $i_{DD_{max}}$ for a falling one). A bell-shaped envelope current with the extracted current as its maximum and the delay of the cell as its width is used as a worst-case approximation. Since signal rise and fall times, pin-to-pin delays and capacitive loads including wiring are already computed in today's cell-based design flows ([8]), only v_X and v_A are left to be determined. An analytical solution for the output signal of a CMOS inverter is given in [9] for two cases listed in Table 1. Assuming a ramp input the output signal is divided into three regions with different dependencies. To keep runtimes low we simplify the dependencies in the three regions. Figure 3 shows the output signal for a rising (falling analog) input ramp applied to a CMOS inverter and Table 2 gives the waveform dependencies of the new T3LEXP model for a *fast* input signal.

fast	:	The input signal reaches V_{DD} $(0V)$ while the n (p) channel transistor is still in saturation.
slow	:	The n (p) channel device leaves the saturation region before the input voltage is V_{DD} $(0V)$.

Table 1: Rising (falling) input ramp criteria

Note that the waveform dependencies of i_X and the noise are derived from v_X (see eqn. (2)). The power waveform is obtained by multiplying v_X and i_X. We assume that the saturation voltage is half the supply voltage. Observing the I-V-characteristic of short channel transistors reveals that this is a reasonable assumption, e.g. [10]. Therefore the condition for a *fast* input can be written as : $t(v_{A_{r,f}} = V_{DD,SS}) < t_{e_{f,r}}$

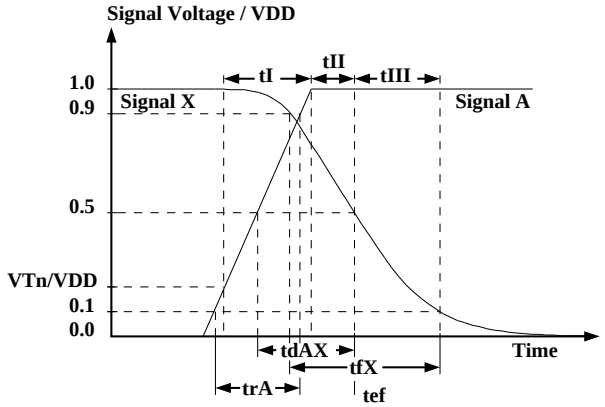

Figure 3: Three regions of a falling signal transition

region	$v_X \sim$	$i_X \sim$	$\frac{di_X}{dt} \sim$	$fast$ input
I	t^3	t^2	t	$t_I = \frac{t_{r,f_D}}{0.8}(1 - \frac{V_{T_{n,p}}}{V_{DD}})$
II	t	1	0	$t_{II} = t_{d_{AX}} - t_{d_{AD}} - \frac{5}{8}t_{r,f_D}$
III	$\frac{1}{1+e^t}$	$\frac{e^t}{(1+e^t)^2}$	$\frac{e^t(1-e^t)}{(1+e^t)^3}$	$t_{III} = p_{f,r} \cdot t_{f,r_X}$

Table 2: T3LEXP Waveform dependencies

The times t_I and t_{II} depend on the rise (fall) time of the driving transistor's gate signal. We denote this signal to D. In the case of an inverter, D is the terminal input A and the rise and fall times t_{r,f_A} are given. For other cells this signal is internal and must be probed for t_{r,f_D} and $t_{d_{AD}}$ during characterization. If t_{II} evaluates to a negative number, a *slow* input was applied. In this case, we just reevaluate t_I using $t_I = t_I + t_{II}$ and set t_{II} to zero. The parameters $p_{r,f}$ are introduced in region III to account for the asymmetry of the waveforms. For large loads case $fast$ applies and the driving transistor conducts the maximum saturation current. In region II the complementary transistor is already off and eqn. (8) holds.

$$I_{SAT_{p,n}} = i_{X_{II}} = V_{DD}\, ln(9)\, \frac{C_X}{4\, p_{r,f}\, t_{r,f_X}} \qquad (8)$$

According to (9) the rise (fall) times are modeled linearly with the load (see [8]), where $t_{0_{r,f}}$ is the rise or fall time at zero load and $K_{r,f}$ is the slope factor.

$$t_{r,f_X} = t_{0_{r,f}} + K_{r,f} \cdot C_X \qquad (9)$$

The intrinsic rise (fall) times $t_{0_{r,f}}$ are very small and therefore negligible for large capacitive loads, hence equation (10) can be derived from (8) and (9).

$$p_{r,f} = \frac{V_{DD}\, ln(9)}{4\, K_{r,f}\, I_{SAT_{p,n}}} \qquad (10)$$

The product of the effective resistance $K_{r,f}$ of a transistor and its saturation current $I_{SAT_{p,n}}$ does not depend on the transistor's size. Therefore, $p_{r,f}$ is constant for a CMOS technology.

4 Implementation

The SPICE simulations are done by a characterization tool we developed for that purpose. All required parameters are extracted in only two simulations per cell-output and stored in a library, which is used by the waveform estimator POWTIM (POWer on TIMe) and the POWer CALculator POWCAL. A gate-level simulator provides the required toggle frequencies and discrete event times during selected time intervals. Using equations (4) to (7) and the T3LEXP model (t^3-linear-exponential) from Table 2, POWCAL and POWTIM calculate the average power or the desired waveform.

5 Model Verification

In this section we will present the capabilities of the new modeling technique by comparing the calculated results to SPICE simulations. Figure 4 shows the

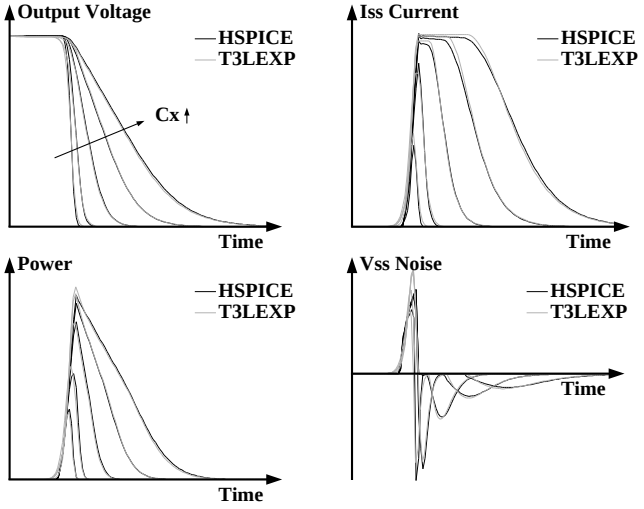

Figure 4: Load dependent waveforms

output voltage, the capacitive current, the power and the noise induced in the V_{SS} line for a falling output signal of a CMOS inverter. The waveforms have been computed for different output loads and are shown together with the results from SPICE. It can be seen that the current waveforms become asymmetric for larger capacitive loads, due to the current limitation of the driving transistor while operating in the saturation region. The differences in the current and power waveforms demonstrate that the power can not be derived from the current only, but by multiplying the current with the drain to source voltage of the corresponding transistor. In case $fast$, the positive noise spike remains constant whereas the negative one decreases rapidly with increasing output load. Figure (5) shows the effect of various input rise times on the waveforms. Here the strong impact of the driving edge on the

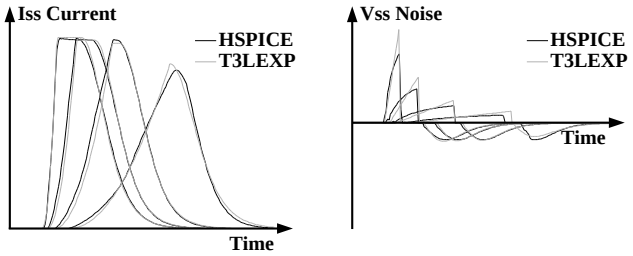

Figure 5: Input rise time dependent waveforms

waveforms in region I is evident. The primary noise spike is decreasing rapidly whereas the secondary one stays constant. Without taking the driving edge into account it is not possible to estimate noise accurately. Besides the edgerate-effect, also the dependency on the output load and the current limitation is covered with the proposed three-region model.

A chain of 9 inverters has been simulated and the results are shown in Fig. 6. Table 3 lists the average, RMS and maximum ratings compared to SPICE results. For the inverter-chain, an error of less than 7% occurred in the estimate of the maximum power.

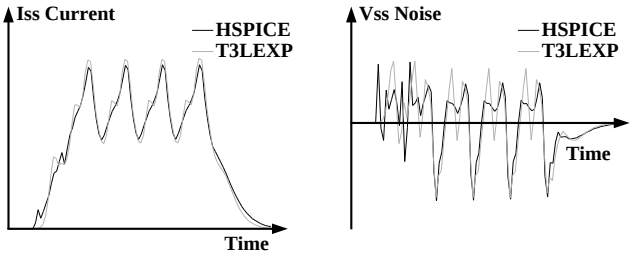

Figure 6: Waveforms for a 9-inverter-chain

	$i_{SS}[mA]$			power$[mW]$			n$[mV]$
source	avg	rms	max	avg	rms	max	max
HSPICE	0.561	0.677	1.176	2.462	3.043	4.615	1.729
T3LEXP	0.564	0.695	1.210	2.607	3.212	4.926	1.768
ERR[%]	0.54	2.66	2.89	5.89	5.55	6.74	2.26

Table 3: POWTIM results for the 9-inverter-chain

To avoid being too pessimistic, the negative feedback of the noise on itself must be taken into account. The primary noise spike reduces V_{DD} (or rises V_{SS}) leading to smaller drain-source voltages, currents and therefore less noise. We take the V_{DD} reduction into account in feeding back the supply voltage of the previous time step as shown in equation (11).

$$V_{DD}\mid_t = v_{DD}(t-\triangle t) - v_{SS}(t-\triangle t) \qquad (11)$$

Figure 7 shows the maximum noise caused in $L = 1nH$ by an increasing number of simultaneously switching $8mA$ output buffers (ON8) discharging a $50pF$ load each. Obviously the noise does not rise linearly due to the negative feedback. Just adding up the noise portions of all cells leads to double the noise for twice the

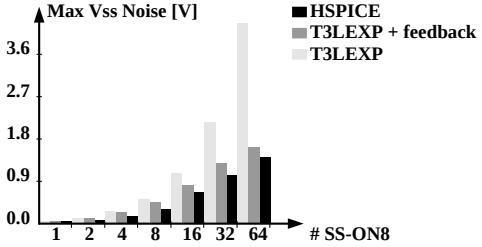

Figure 7: Nonlinear noise due to negative feedback

number of simultaneously switching output buffers. As can be seen, this grossly overestimates the actual noise. The nonlinearity is matched much better by POWTIM that takes the feedback into account.

6 Experimental Results

After we have examined the accuracy on the cell level, we will now show results on a number of designs from the ISCAS'85 and '89 benchmark suites. Since no simulation vectors are available for these designs, we resort to random vectors. The numbers shown in Table 4 give the average, RMS and maximum power and noise calculated by POWTIM and HSPICE^{TM} for the critical cycle (the one with the largest number of events). The simulations were performed with $10MHz$ frequency using VERILOG^{TM}.

circuit		power $[mW]$			noise $[mV]$		cpu[s]
name	source	avg	rms	max	min	max	
c95	HSP	3.361	8.414	32.40	-0.39	0.373	119
	PT	3.434	8.509	33.30	-0.42	0.333	2
	ERR	2.17	1.13	2.76	7.11	-10.7	-
c880	HSP	37.63	66.55	155.0	-2.70	3.438	2854
	PT	43.33	77.82	232.6	-2.42	3.579	19
	ERR	15.15	16.94	50.06	-10.4	4.10	-
c2670	HSP	155.3	236.3	571.9	-9.74	7.684	13219
	PT	160.2	250.7	694.4	-6.88	9.249	63
	ERR	3.17	6.11	21.43	-29.3	20.37	-
c3540	HSP	152.3	207.2	475.9	-4.94	6.840	23051
	PT	200.9	250.2	570.3	-6.51	8.706	83
	ERR	31.89	20.75	19.85	31.76	27.28	-
s27	HSP	1.389	4.353	25.98	-0.71	0.642	146
	PT	1.317	4.355	29.53	-0.80	0.736	3
	ERR	-5.18	0.05	13.67	12.29	14.64	-
s298	HSP	8.208	21.19	102.0	-4.14	3.271	2008
	PT	8.704	22.94	106.5	-4.09	3.749	8
	ERR	6.04	8.25	4.40	-1.19	14.61	-
s444	HSP	7.370	20.59	116.7	-6.58	4.143	1842
	PT	8.398	23.51	117.4	-5.29	4.891	7
	ERR	13.95	14.21	0.57	-19.5	18.06	-
s713	HSP	14.88	33.07	168.8	-7.16	3.410	3870
	PT	15.19	33.51	212.2	-7.36	5.469	15
	ERR	2.06	1.33	25.71	2.82	60.38	-
mean error		9.95	8.60	17.31	14.30	21.27	-

Table 4: POWTIM (PT) results for maximum cycle

In average, the maximum power and noise values are overestimated by 17% and 21% respectively. The

error varies from 0.6% for the maximum power of circuit s444 to 60.4% for the maximum noise of circuit s713. Averaging the waveforms deviates less than 10% from the SPICE numbers, varying from 2.1% to 31.9% for the power of circuits s713 and c3540. Figure 8 shows a comparison between the calculated supply current transients and the ones simulated by SPICE. The clocking scheme was chosen such that the rising clock edge occurs first, followed by the falling one together with the input data. Circuit s713 experiences

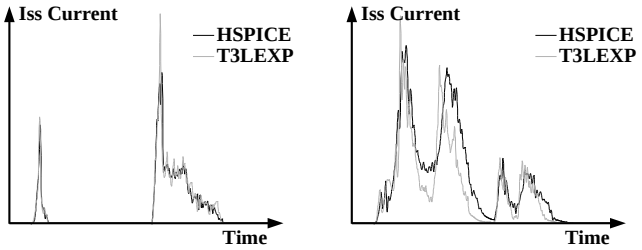

Figure 8: Supply currents for s713 and s1411

the most activity after the falling clock edge when the inputs are switching and circuit s1411 needs nearly half the cycle to compute its next state. Also, the large one experiences two maxima whereas the smaller one shows the typical behavior of fast decaying activity. In general the waveforms computed by POWTIM match the SPICE results. The differences are due to the assumptions in the model and due to errors in the estimated delays and edgerates. Besides the dynamic waveforms, the average power was calculated by POWCAL for all vectors and the critical cycle only using the following four modeling techniques :

A, modeling technique described in [11]
B, output capacitances are taken into account only
C, internal capacitances are added to output loads
D, equation (6)

circuit			max cycle avg power $[mW]$				all
name	gates	events	A	B	C	D	D
c95	50	20	6.188	2.637	2.905	3.295	2.037
c880	556	484	43.91	28.67	33.14	43.36	18.01
c2670	1687	1748	178.7	107.5	126.7	162.5	86.26
c3540	2424	2219	225.4	131.7	155.0	201.1	106.4
s27	40	18	1.857	0.810	1.246	1.497	0.903
s298	325	116	13.49	4.367	7.004	8.511	3.884
s444	490	116	10.66	3.879	6.654	8.325	5.042
s713	687	299	17.36	9.679	12.51	16.12	8.919
mean error [%]			35.59	-34.05	-12.64	10.79	-

Table 5: Average power for max. cycle and all vectors

From columns B and C it can be seen that taking only capacitances into account significantly underestimates the power by 34.05% and 12.64% in average. While modeling technique A is too pessimistic, D correlates to the power waveform average calculated by POWTIM and the power average simulated with SPICE. In the last column of Table 5, the average power dissipation for all 10000 random vectors is given also. The large deviation between the global average and the average of the critical cycle shows that the power is highly pattern dependent.

In order to find out if this is true also for large circuits stimulated with functional input vectors, some industrial designs are analyzed next. The simulations

circuit		average power $[W]$			error [%]		cpu $[s]$
name	♯gates	func	rand	meas	func	rand	PC
lc1	$5K$	0.159	0.154	0.146	8.90	5.48	3
lc2	$8K$	0.136	0.159	0.127	7.09	25.2	5
lc3	$10K$	0.458	0.456	NA	-	-	9
lc4	$50K$	1.570	1.307	1.473	6.59	-11.3	42
lc5	$85K$	0.423	0.446	0.418	1.20	6.70	60

Table 6: POWCAL for large designs (all vectors)

circuit		max cycle avg power $[W]$			cpu$[s]$
name	♯events	func	rand	error [%]	PT
lc1	1359	0.221	0.306	38.46	83
lc2	1066	0.146	0.174	19.18	54
lc3	3250	0.562	0.903	60.68	182
lc4	17961	1.632	1.517	-7.05	1008
lc5	11226	0.795	0.944	18.74	591

Table 7: POWTIM for large designs (max cycle)

were done with real application vectors that have been used to measure the power consumption on a tester. Tables 6 and 7 show the results and the corresponding runtimes. For all circuits the average deviation to the measured power is 6% for the functional pattern and 12% for the random vector sets. The power of the worst-case cycle is overestimated by 30% in average using random vectors. Only circuit lc4 is always underestimated when random vectors are simulated. This indicates that the behavior of a circuit stimulated by random vectors is unrealistic. Figure 9 shows the runtime of POWCAL and POWTIM for analyzing the

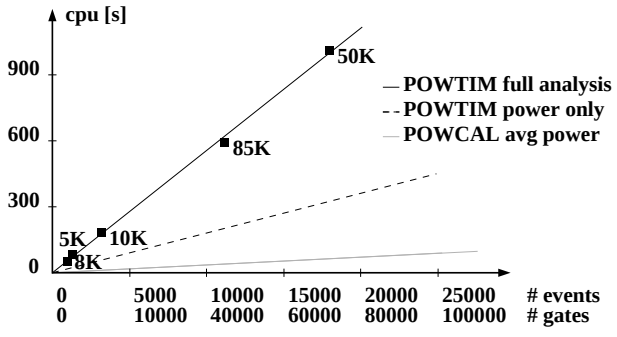

Figure 9: CPU time of POWCAL and POWTIM

circuit	power (all vec.) [W]			core power [%]		
name	total	I/O	core	clock	ff	logic
lc1	0.159	0.085	0.074	20.3	51.3	28.4
lc2	0.136	0.003	0.133	32.3	65.4	2.3
lc3	0.458	0.026	0.432	10.0	19.0	71.0
lc4	1.570	0.072	1.498	17.7	50.9	31.4
lc5	0.423	0.014	0.409	20.0	53.0	27.0

Table 8: Power distribution on circuit components

worst-case cycle. It can be seen that the complexity of POWTIM (POWCAL) is linear with the number of events (gates), allowing 85K gates to be processed in 10 (1) cpu minutes only.

Table 8 shows how the power is distributed among the core and the I/O area. For most of the designs the clock tree consumes 20%, the flip-flops 50% and the combinational logic around 30% of the power. In circuit lc2 the sequential power dominates with a 65% share and in circuit lc3 most of the power (71%) is consumed in the combinational logic. The power consumption of the I/O cells is between 2% and 6% of the total power consumption for most circuits. A notable exception is circuit lc1 which consumes half the power in the I/O area. This points out that the total power consumption and the distribution of the power is highly design and pattern dependent. Therefore the circuits must be stimulated with functional pattern, emulating the usage of the chip in the system it is designed for, in order to get realistic and reliable results.

7 Conclusion

We have developed a methodology to characterize cells for average and time dependent power consumption, supply current and noise. A black box modeling approach was chosen, partly simplifying the problem to tackle large circuits. To keep the accuracy within 10%, simplifications were made where appropriate and a large modeling effort was spent in areas with significant influence on the current flow in an IC. Gate level logic simulation was employed to get the required number of signal changes and discrete event times during selected time intervals.

The models have been verified against SPICE results on cell and circuit levels over a wide range of parameters for a commercial submicron technology. We significantly improved the calculation of the time dependent capacitive power by multiplying the capacitive current with the signal voltage and not the constant supply voltage. Due to the consistent modeling of the noise and the capacitive current as derivatives of the signal voltage, the resulting waveforms are electrically correct and match data generated by computationally much more expensive SPICE simulations. Since the gate-signal's fall (rise) time of the transistor that charges (discharges) a capacitive load is included in the model of a cell, we are able to account for the high sensitivity of the primary noise spike on this parameter. Also, the significant influence of the negative feedback of the noise has been shown and is taken into account for the first time. In addition to the transient waveforms, both average and RMS currents are computed to support electromigration MTTF calculations. The average power and its distribution to different portions of the design is reported. This helps the designer to find out where the power is consumed in order to do appropriate design changes if the power needs to be reduced. The short runtimes and the high accuracy that has been achieved for some large designs prove the linear complexity and applicability of our event driven approach. It can be used within a higher level reliability verification system (as proposed in [12]) and to iteratively optimize a circuit until the current, noise and power constraints are met.

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