Clock Grouping: A Low Cost DFT Methodology for Delay Testing*

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Abstract

A low overhead DFT technique, called clock-grouping, for delay testing of sequential synchronous circuits is presented. The proposed technique increases robust path delay fault coverage for circuits by exercising greater control over flip-flop clocks in the test mode. In the test mode, the flip-flops are partitioned into different clock-groups. The flip-flops in each clock group can be either clocked or not clocked, independent of the flip-flops in the other groups. This flexibility is used to enhance the number of different (v_1, v_2) test pairs that can be applied to the state inputs of the circuit thereby increasing coverage of delay faults. Experimental data on benchmark circuits shows that high fault coverage can be obtained by using only two clock groups in most circuits.

The proposed clock grouping methodology can be applied to non-scan circuits as well. In fact, it can provide a DFT solution for high speed data path circuits where the performance penalties of conventional DFT techniques are unacceptable.

1 Introduction

Growing circuit speeds are making it essential to test circuits for delay faults. With the use of aggressive statistical timing, a certain fraction of manufactured chips fail to perform at the desired clock rate. With the popularization of MCM technology, it is becoming imperative to ensure that the dies are not only free of any logical failures, but are also guaranteed to perform at the specified clock rates. The general concern for improving quality of the shipped products is also leading to the popularization of delay testing.

Delay testing differs from the conventional (stuck-at) testing significantly since it requires two pattern tests (v_1, v_2) [6, 14]. The initialization vector (v_1) is applied to the circuit to obtain desired initial values at various circuit nodes by charging/discharging the node capacitances. The test vector (v_2) is then applied to launch the desired transition to a circuit output. Under path delay fault model [6, 14] the transition is created along the target path, starting at a primary (state) input and ending at a primary (state) output. A (v_1, v_2) pair is said to be a robust test for a given path delay fault if cannot be invalidated by any other delays in the circuit [6]. The application of two pattern test (v_1, v_2) at inputs to the combinational logic should be hazard free.

Design for testability (DFT) techniques to enable comprehensive delay testing of synchronous sequential circuits differ significantly from the scan (or partial scan) techniques employed for stuck-at testing. The need to apply two-pattern tests at inputs of the combinational logic, hazard free, adds new dimensions to the DFT problem. This paper presents a low cost DFT methodology which enables the application of desired test patterns to the circuit inputs. We begin by a discussion of existing DFT methodologies for delay testing.

It was proposed in [7] that the scan chain be enhanced by the use of additional hardware to enable shifting in any desired v_1 as well as v_2, for each state input of the circuit. However the area overhead of this scheme is very high. Recently, two main test application strategies have been considered. The first one is called functional justification (e.g. see [2]). In this scheme, the circuit flip-flops are designed as in conventional scan design for stuck-at testing. In the test mode, the flip-flops are configured as a scan chain to shift in a desired v_1 at the state inputs of the circuit. The circuit nodes are then allowed to stabilize to their steady state values. The flip-flops, now configured in functional mode, load the next-state output of the circuit. Appropriate primary input values, along with the values loaded in the flip-flops, constitute v_2. Clearly, v_2 applied to the state inputs to the combinational logic depends on v_1 and the next state logic of the function. In this mode, if the next state of the circuit for a given v_1 matches the desired v_2, then the fault is detected. It was reported in [1] that most untestable path delay faults in sequential circuits are not robustly testable due to the incompatibility between the next state output for input v_1 and the value required at state inputs by v_2.

The other mode for test application also employs conventional scan design. It is called scan-shifting [2] or skewed-load [11, 12, 13]. In this test application mode,

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Figure 1: Circuit with Clock Groupi

be useful both under the functional justificatio
scan-shifting modes of two pattern test applic
perimental results show significant improvem
coverage without the use of extra latches. A sr
of groups is typically sufficient to improve th
of the circuit significantly.

The overhead of the clock grouping DFT m
over conventional scan design, is minimal. I
to small modifications in the clock distribut
tra pins for the test clock signals. Typically
accomplished in much lower overhead than th
use of extra flip-flops in the scan chain.

Though scan is assumed in the followin
of clock grouping is useful for testability en
whether or not scan is employed. In non-sc
clock grouping can be used to achieve higher
age not only due to its capability to apply a la
of v_2 vectors for any given v_1, but also by enab
plication of a larger set of initialization vector
In fact, in high speed data path circuits (tha
ple control structure), the application of clo
can provide a DFT methodology for compreh
testing *with no performance penalty.*

In the following, the circuit under test ((
sumed to be synchronous sequential circuit wi
It is assumed that the flip-flops can hold th
for at least two consecutive clock cycles if t
clocked. It is further assumed that the scan c
to scan in any desired v_1. Since, any desire
values can be applied at the primary inputs,
that of application of appropriate v_2 values
inputs. There are three different ways to obta

Figure 2: Example for Pa

The above example illustrate
tively clocking flip-flops to appl
state inputs in v_2 are not compa
output for v_1. In the limit, eac
individually controlled for test a
the area overhead for such a de
practical reasons, the flip-flops i
to be grouped into k groups wher
ing discussion, $\{D_1, D_2, \ldots, D_l\}$
flops. $\{y_1, y_2, \ldots, y_l\}$ are the (p
the combinational circuit corresp
these flip-flops. Finally, $\{Y_1, Y_2, .$
outputs of the combination circu
inputs to the flip-flops. The cloc
now be stated.

Problem Statement Determ
flip-flops to maximize the num
that can be tested by applying a
signal to each group.

There are 2^k different clock/nc
sible under k clock groups. Of t
responds to the hold mode and
tect delay faults in the paths sta
Also, the all clock case correspond
functional justification mode. H
into k groups allows $2^k - 2$ new
rations. Test application using
shall be called *partial functional*

Clock Grouping Procedure
shown in Figure 2 (b) again. Th
sired two-pattern test requires th
clocked, while flip-flop D_2 must
dicates that for the application
D_1 and D_2 must belong to differe
can be grouped with either flip-
cate the i-th bit of v_1 (v_2). Note

Figure 3: Reduced correlation d

4 Scan Shift with Clock

In this section, it shall be show
very useful even with scan-shift m
In scan shift mode, scan chain is
the flip-flops. After the combinatio
at its steady state value under in
the scan chain are shifted by one
inputs for v_2. Simultaneously, app
plied at primary inputs.

For any given v_1, only a subset
can be applied at the state inputs
to the outputs of the flip-flops in t
if v_1 (for state inputs) is fully sp
different v_2 values can be applied
Even these two v_2 values differ o
connected to the flip-flop output t
scan-in pin. This correlation bet
state inputs is a major cause for ob
coverage. Many techniques have b
erature for ordering flip-flops in th
fault coverage [2, 9, 13]. Note that
tra flip-flops is typically required
path delay fault coverage. Our ob
impact of clock grouping on the fa
by the scan shifting test applicatio
follows shows how clock grouping c
relation at low hardware overhead

4.1 Scan Correlation and

Consider state inputs y_i and y_j
tive flip-flops on the scan chain. As
of the following discussion that the
y_j in both v_1 and v_2 are fully spe
lustrates the nature of the correla
possible fully specified values can
in this configuration. Only those
applied that have $v_{1i} = v_{2j}$. It is
flip-flop that precedes D_i can pro

then all 8 different two pattern combinations can be applied to y_i and y_j as shown before. However, if D_i is clocked while D_j is not, it is possible for y_j to retain its old value. Hence, by this scheme, 12 (out-of 16) two pattern combinations can be applied to the inputs y_i and y_j. Now two pattern tests that have $v_{2j} = v_{1j}$ can be applied, even when $v_{2j} \neq v_{1i}$. (Note that it is again assumed that the flip-flop that precedes D_i in the scan chain can provide the required bit value for v_2 for y_i.) This reduced correlation due to clock grouping can drastically improve pattern pair coverage at the inputs that belong to same outputs but the corresponding flip-flops must be assigned consecutive stages in the scan chain. It can be easily shown that the test patterns that can be applied to the circuit inputs under multiple clock groups are a super-set of the patterns that can be applied using full scan-shift. Given k-clock groups, 2^k different clock/no-clock combinations can be used. If none of the clock groups are clocked between the application of v_1 and v_2, then it corresponds to the hold mode. If all the groups are clocked, then we get the conventional *full scan shift* case. The remaining $2^k - 2$ cases are called *partial scan shift*.

4.2 Design Procedure

At this stage, the order of flip-flops in the scan chain and clock grouping may need to be determined. In either case, the delay faults in paths originating at primary inputs and the delay faults in the paths starting at state inputs that are detected by full functional justification can be eliminated from consideration. Two main scenarios are considered.

Partial Functional Justification The full functional justification can be followed by clock grouping to maximize extra fault coverage obtained by partial functional justification. The faults detected by partial functional justification are dropped from the fault list. ATPG is used to generate tests for the faults remaining in the fault list. A scan chain ordering procedure has been developed that takes into account the difference between the set of possible two pattern values that can be applied to the successive flip-flop outputs depending on whether the two flip-flops belong to the same or different clock groups. A greedy heuristic is used to determine chain order to maximize the number of path delay faults that can be detected by using full and partial scan-shift modes.

Partial Scan Shift In this case both clock grouping and scan chain ordering need to be performed. The fault list contains all SI paths that are not detected by full functional testing. ATPG is used to generate two pattern tests for the faults in the fault list. Only those patterns that can be applied using scan-shifting are retained. Then a procedure similar to the one used in [2] is used to determine the order of flip-flops in the scan chain. The faults detected by full scan-shift are eliminated from the fault list. The clock grouping is then performed using the remaining test vectors to maximize the additional fault coverage obtained by partial scan-shift (the procedure is similar to the one outlined for partial functional justification). Finally, the ATPG uses the given clock grouping to generate partial functional justification tests to determine the overall fault coverage. The experimental results for both these cases are presented next.

Table 1: Fault Coverage under 1,2 and 3 Clock Grouping

Circuit		*Clock Grouping Using Partial*			
		F.J.		*S.Shifting*	
Name	*1 Grp*	*2 Grps*	*3 Grps*	*2 Grps*	*3 Grps*
s27	90.9	100	100	100	100
s208	61.3	75	84.4	73.6	84
s298	73.8	95.6	94.3	86.4	93.7
s344	81.4	90.3	93.5	91.9	94.9
s349	81.4	90.3	93.5	91.9	94.9
s400	76.8	73	93.1	87.8	92.8
s420	71.8	76.8	84.2	80.2	87.5
s444	74.6	96.2	97	86.3	91.9
s510	39.8	65.6	80.6	61.9	74
s641	84.1	95.2	98.2	94.4	96.8
s820	48.4	73.6	81.6	69.4	81.2
s953	99.9	100	100	99.9	100
s1196	100	100	100	100	100
s1238	100	100	100	100	100
s1488	36.3	70.6	84.3	66.4	82.3
s1494	36.1	70.3	84.3	66.4	82.5

5 Experimental Results

In this section, the experimental results shall be presented for ISCAS 89 benchmark circuits for the two cases described above. In both the cases, only the delay faults in paths originating at state inputs are considered. Tests are applied under full and partial, functional justification as well as scan shifting. However, the two cases differ in the way the clock grouping and scan chain ordering are determined. In the first case, the scan chain ordering is determined mainly from considerations of partial functional justification. This is followed by scan chain ordering. In the second case, the scan chain ordering is performed first. The clock grouping is then determined mainly to maximize the coverage of remaining delay faults via partial scan shifting.

First consider the case without the application of clock grouping DFT methodology. Without clock grouping only full functional justification and full scan shift can be used (in addition to the hold test application mode). After ordering the scan chain, the total fault coverage obtained for various benchmark circuits is as shown in Table 1 (column marked *1 Grp*). Fault coverage is very low for many circuits. (All results presented here are for the SI paths only. Further, the fault coverage is computed as a percentage of all faults for which ATPG found a two pattern test.)

Partial Functional Justification Table 1 (columns marked *F.J. — 2 & 3 Grps*), presents the fault coverage information for two and three clock groups, respectively. The use of clock grouping (even two clock groups) provides a significant increase in fault coverage over the case without clock grouping. For many circuits (s298,

s344, s349, s444, etc.) the fault coverage is very high for two clock case. Further, circuits such as s510, s1488, and s1494, that had extremely low fault coverage without clock grouping, had significant improvements. Note that these circuits otherwise require *one extra flip-flop for each circuit flip-flop* to obtain high fault coverage (e.g. see data in [2]). The fault coverage increased further when three clock groups are used. However, the increase in fault coverage over two clock case is lower. The overall fault coverage is very high for most circuits.

Partial Scan Shift The clock grouping provides significant increase in fault coverage over the single clock, even with two clocks Table 1 (columns marked *S.Shifting*). For some circuits, higher fault coverage was obtained over the previous case. Use of three clock group further increases the fault coverage as well.

The results obtained by the application of the proposed clock grouping technique show that significant improvements can be obtained in fault coverage by clock grouping. In most cases, grouping circuit flip-flops into just two or three groups can provide high fault coverage. Also, it was found that many circuits that would otherwise require doubling the number of flip-flops to obtain high fault coverage, can be tested very comprehensively by the application of clock grouping technique. It was also observed that in most cases, higher fault coverage was obtained by performing clock grouping for partial functional justification than for partial scan shift. An algorithm that can perform scan chain ordering and clock grouping for partial scan shift simultaneously is currently being developed.

6 Conclusion

A low overhead DFT technique, called clock-grouping, for delay testing of sequential synchronous circuits is presented. The proposed technique increases robust path delay fault coverage for circuits by exercising greater control over flip-flop clocks in the test mode. In the test mode, the flip-flops are partitioned into different clock-groups. The flip-flops in each clock group can be either clocked or not clocked, independent of the flip-flops in the other groups. This flexibility is used to enhance the number of different (v_1, v_2) test pairs that can be applied to the state inputs of the circuit thereby increasing coverage of delay faults. Experimental data on benchmark circuits shows that high fault coverage can be obtained by using only two clock groups in most circuits.

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