A Multi-objective Approach to Configuring Embedded System Architectures

James Northern and Michael Shanblatt

Department of Electrical and Computer Engineering
2120 Engineering Building
East Lansing, MI 48824-1226
jnorthern@xula.edu, mas@msu.edu

Abstract. Portable embedded systems are being driven by consumer demands to be thermally efficient, perform faster, and have longer battery life. To design such a system, various hardware units (*e.g.*, level one (L1) and level two (L2) caches, functional units, registers) are selected based on a set of specifications for a particular application. Currently, chip architects are using software tools to manually explore different configurations, so that tradeoffs for power consumption, performance, and chip size may be understood. The primary contribution of this paper is the development of a novel power-performance design tool based around a core GA search and optimization technique. The tool targets the implementation of portable embedded systems.

1 Summary

This paper presents a framework for an evolutionary computational approach to configuring an "ideal" embedded processor based on power consumption and performance. In addition, a database of simulation results that gives a more comprehensive evaluation of tradeoffs between power, performance, and inter-dependence between parameter configurations (*i.e.*, L1 to L2 cache size, memory bandwidth, instruction window size, datapath width) is presented. Appropriate search techniques to reduce exploration space and decrease time-to-market are also discussed.

Power and performance trade-offs are evaluated through the use of Pareto-optimal analysis, for benchmark designs. The experiments used estimated values with a targeted workload (*test-math.c* and *126.gcc*) for power consumption and cycles per instruction (CPI) per configuration. The fitness function was varied based on a weighted scale, where power or performance is selected, with a 100% weighted value, and as 50% power and 50% performance to gather a mixture of both objectives to guide the search process. Five initial randomly seeded populations were submitted to the GA for diverse exploration of the search space. The population size for each run was 50, with termination set at a maximum of 50 generations. A single-point crossover rate of 30%, and mutation rate of 1.4% was used for reproduction operators. The selection scheme for new chromosomes was stochastic universal sampling using linear scaling of fitness values.

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A comparison of published performance and maximum power for three processors is presented. These three processors are from MIPS, Wattch, and a study done at the University of Pennsylvania [1,14]. The first configuration is the MIPS processor taken from the R10000 specifications [1]. The second configuration is a baseline model for a high-end processor taken from the Wattch simulator toolset [1]. The third configuration is taken from a study done at the University of Pennsylvania (PENN), which demonstrated different tradeoffs between configurations for improved performance. The first two configurations used out-of-order processing, while the last configuration used in-order processing. The in-order processing improves power efficiency, but increases CPI performance. Since performance is the leading objective for these examples, the original configuration is taken from the best solution in the first generation of solutions for performance optimization. The results are expressed as a percentage of the original designs' power consumption and CPI performance. The percentage illustrates the improvement in power consumption and performance for conventional designs and those derived through the GA optimization tool.

However, for each GA run the other objective suffered. With performance being the main objective in the case of the math benchmark, the calculated power consumed showed a decline of 125% in comparison to the original best configuration. The industry example, MIPS R10K simulated processor showed an improvement of 14.19% in power consumption, but a 26.69% decline in CPI performance in comparison to the original configuration. In comparison with the other specified processor configurations, the R10K trades power consumption for higher performance. The Wattch example showed an improvement of 30.09% in power consumption, but a 14.67% decline in CPI performance. The Wattch example considers both power and performance for an overall better processor. Again, the configuration used in a study from the University of Pennsylvania showed lower performance and better power savings in comparison to the other examples.

In the case of the GNU C compiler benchmark, the architecture was optimized for power and the maximum amount of savings was 34.71% with a 10% increase of performance. Using the multi-objective search, we were able to select a configuration with improved power consumption of 49.17%, sacrificing performance with a gain of 1%. The total in power-performance savings was ~50% compared to single-objective optimization total of ~45%.

References

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[2] Roth, A., online at http://www.cis.upenn.edu/~amir/cis501-01, CIS 501: Introduction to Computer Architecture, University of Pennsylvania, 2001.