System Level Signal and Power Integrity Analysis Methodology for System-In-Package Applications

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ABSTRACT

This paper describes a methodology for performing system level signal and power integrity analyses of SiP-based systems. The paper briefly outlines some new modeling and simulation techniques that have been developed to enable the proposed methodology. Some results based on the application of this methodology on test systems are also presented.

Categories and Subject Descriptors

J.6 [**Computer-Aided Engineering**]: *Computer-aided design*

General Terms

Design

Keywords

Causality, modal decomposition, nodal admittance matrix method, power integrity, signal integrity, System-In-Package (SiP), finite difference method.

1. INTRODUCTION

The increasing performance and miniaturization requirements in the electronics industry have resulted in an underlying trend towards convergent systems. Such systems bring about functional integration and reduction in size through a variety of technology platforms like system-on-chip (SoC), multi-chip modules (MCM), system-in-package (SiP) etc., depending on which is most suitable for the application. Among these technologies, SiP provides a platform for integration of multiple dies and passives onto a single package using a range of technologies from new materials and processes to novel designs and techniques. Figure 1 shows the schematic diagram of a SiP with integrated RF / Digital, embedded passives and electromagnetic band gap (EBG) structures. Such SiP based structures considerably increase the system complexity thereby giving rise to new signal and power integrity problems. To deal with these issues requires new EDA tools and techniques that can: 1) accurately model and analyze complex SiP structures, 2) accurately simulate the parasitic effects in the system, and 3) efficiently handle large sized problems so as to enable system level analysis and simulation. This paper describes a methodology for performing system level signal and power integrity co-simulation of SiP based systems. The paper also briefly outlines some new modeling and simulation techniques to enable the proposed methodology.

Section 2 outlines a novel methodology for signal – power co-simulation. Section 3 describes the analysis of power distribution network (PDN) using a circuit based finite difference modeling technique. Section 4 describes the integration of the PDN and the signal distribution network (SDN) using the nodal admittance matrix and modal decomposition techniques. Section 5 describes the delay extraction technique and the simulation of the integrated system response using signal flow graphs. The results obtained using the proposed methodology on a test structure are discussed in section 6. Finally, the conclusion along with some considerations is presented in section 7.

2. PROPOSED METHODOLOGY

Traditionally, in packaged systems the analyses of the SDN and the PDN have been carried out independently. Once the layout of a system is available, geometrical information is extracted to obtain models for the PDN and the SDN separately. However, it is known that simultaneous switching noise (SSN) in the PDN can affect the quality of the signal that propagates through the SDN. Analyzing the two networks separately fails to account for these effects accurately and hence, compromises on the quality of the SI analysis. In mixed signal systems, where milli-volt amplitude levels matter, the co-simulation becomes extremely critical. One possible solution for this problem is using macro-modeling [1] along with model order reduction to convert the frequency domain

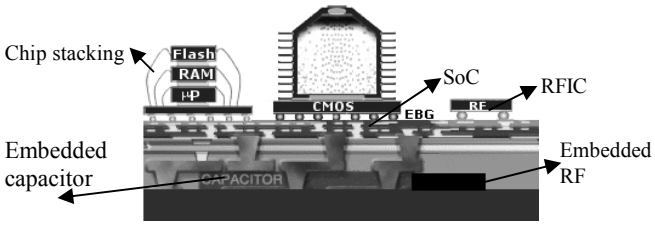


Figure 1. Schematic diagram of a system- in-package (SiP)

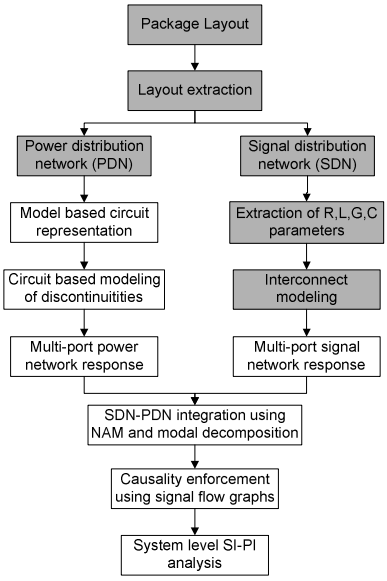


Figure 2. Proposed methodology for system level SI-PI analysis

response of a PDN into a SPICE compatible format that can be combined with SPICE based SDN models to carry out a system co-simulation. However, macro-modeling has its own limitations. Typically, macro-modeling requires some function based approximation of the frequency response data which limits the size of the problem (in terms of ports and bandwidth) that can be handled. Furthermore, macro-models obtained using bandlimited frequency response data are unable to accurately capture distributed effects like delay leading to causality violations in the transient simulations [2]. Another problem with this macro-modeling approach is that the PDN analysis is typically done using EM solvers. This is extremely time consuming and limits the size of the structures that can be simulated. To address this problem, several circuit based modeling techniques have been proposed in literature to reduce the PDN simulation time [3]. The methodology proposed in this paper (shown in Figure 2) provides an efficient and reliable way of analyzing SiP structures by using novel modeling and simulation techniques. The initial steps in the methodology (shown using shaded boxes) use existing techniques

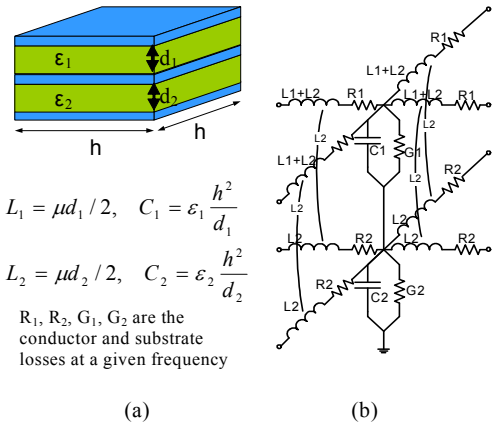


Figure 3. (a) Geometry and p.u.c. parameters. (b) Combined unit cell model for three planes.

for layout extraction and interconnect modeling. However, the proposed methodology uses a modified modeling approach for analyzing the PDN. The approach accurately models structural discontinuities and is able to extract multi-port response of the PDN. The PDN and SDN responses are then integrated using the nodal admittance matrix (NAM) method and modal decomposition techniques. This ensures that all the coupling between the SDN and the PDN is accurately captured in the simulation. The integrated system response is then transformed to obtain a reduced-order model of the system. This reduced order model captures all the system parasitics and can be efficient simulated using signal flow graphs. The signal flow graph formulation includes a delay extraction technique that enables the enforcement of causality on the transient simulation.

3. ACCURATE NAM BASED MODELING OF THE PDN

In the past, circuit-based techniques have been proposed as a replacement to 3D full-wave analysis of package PDNs [3], which is computationally expensive. These circuit techniques are based on the finite difference frequency domain (FDFD) solution of the Helmholtz equation. A given PDN structure can be meshed into a grid of square "unit cells".

Figure 3 shows how an elemental unit cell of a three metal layer structure can be decomposed into an equivalent circuit. A PDN can thus be represented by a circuit, which can then be solved to obtain the multi-port frequency response. Complex irregular geometries can be handled by modifying individual unit cells. More information behind this technique is provided in [3][5]. Extensions to this technique in order to model discontinuities such as the edge effect and slots in the plane have been proposed

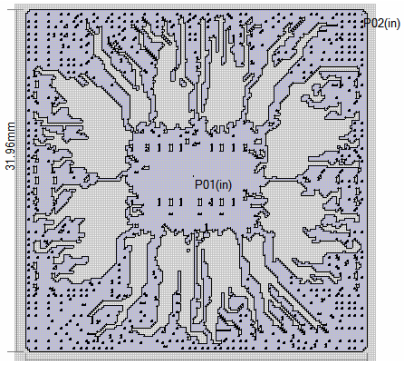


Figure 4. Example FDFD model of a package structure

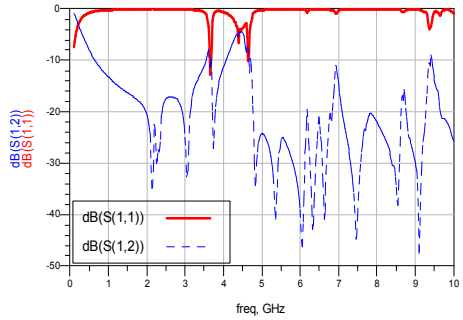


Figure 5. Simulated S parameters for the Package layer of Fig. 4

in [6]. With increasing integration of EBGs and split planes, these models gain significance in a mixed signal SiP environment. An example of a meshed model for a SiP layer is shown in Figure 4. This example contains approximately 25,000 nodes and the frequency response, from 0.1 GHz to 10 GHz was obtained in 84.3 seconds using the method described in Figure 3[5]. The S parameters between ports 1 and 2, defined between the center and one of the corners, are shown in Figure 5.

4. INTEGRATION OF THE SDN AND THE PDN

Since separate analyses of the SDN and the PDN fails to account for the coupling between the two domains, the two responses need to be integrated to perform an accurate system level analysis. This integration can be performed using the admittance matrices of the two modules along with the stamp rule [7]. The process involves conversion of the SDN response into its equivalent model which is then stamped onto the admittance matrix of the PDN. For example, in Figure 6, a microstrip transmission line referenced to non-ideal power ground planes is replaced with the model shown in Figure 7. This model is then stamped on to the admittance matrix of the power/ground planes by taking into consideration the appropriate modal decomposition technique. This ensures that all parasitic effects between the PDN and the SDN are accurately accounted for in the integration process. For example in a simple microstrip interconnect referenced to non-ideal power ground planes (see Figure 6), since the transmission line and parallel-plate modes are not coupled, the integration of the SDN and the PDN responses can be carried out simply by combining the two Y-matrices as given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} Y_p & 0 \\ 0 & Y_m \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \quad (1)$$

where Y_p and Y_m are the Y-matrices of the power/ground planes and the microstrip interconnect (considering ideal reference) respectively, while I and V are the vectors defining the currents and the voltages at the input and output ports. However, if the current on the signal line excites both modes, like in the case of a stripline interconnect referenced to non-ideal power/ground planes, additional considerations [8] are required to integrate the SDN and the PDN responses. For the stripline case, the SDN and the PDN responses can be integrated as given by

$$\begin{bmatrix} I_p^i \\ I_p^o \\ I_m^i \\ I_m^o \end{bmatrix} = \begin{bmatrix} k^2 Y_s + Y_p & kY_s \\ kY_s & Y_s \end{bmatrix} \begin{bmatrix} V_p^i \\ V_p^o \\ V_m^i \\ V_m^o \end{bmatrix} \quad (2)$$

where Y_p and Y_s are the Y matrices of the power/ground planes and the stripline (considering ideal reference) respectively, and k is a constant determined from the layout.

Once the integration is complete, the line terminations and the other lumped components in the system can be added to the overall system matrix using the stamp rule. Since the transient response is often required only at particular locations in the system, the overall system matrix can be reduced to include ports only at those locations where the system is being excited or probed. The reduced system matrix thus obtained is then used for estimating the port-to-port delays in the system to enforce causality on the transient response.

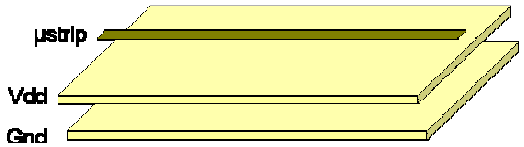


Figure 6. A microstrip-line referenced to a non-ideal power-ground plane

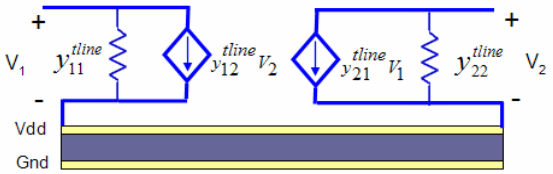


Figure 7. Equivalent two port model of microstrip line

5. CAUSAL TRANSIENT SIMULATION USING SIGNAL FLOW GRAPHS

The reduced multi-port Y-parameters are converted to S-parameters for simulation using signal flow graphs (SFGs). A novel technique for extracting port-to-port delay from the frequency response of a passive structure is proposed in [2]. The technique makes use of the minimum-phase property of passive systems in conjunction with the Hilbert transform and involves the separation of the transfer responses of a system into minimum phase and all-pass components. Based on the theory described in [2], if Td is the port-to-port delay for a 2-port passive network described by its S-parameters, the delay extraction process can be described as follows:

$$|S12_{\min}(j\omega)| = |S12(j\omega)| \quad (3)$$

$$\arg[S12_{\min}(j\omega)] = -\frac{1}{2\pi} \mathrm{P} \int_{-\pi}^{\pi} \log|S12(j\theta)| \cot\left(\frac{\omega-\theta}{2}\right) \quad (4)$$

$$S12_{AP}(j\omega) = \frac{S12(j\omega)}{S12_{\min}(j\omega)} = e^{-j\omega Td} \quad (5)$$

$$Td = -\frac{\arg(S12_{AP}(j\omega))}{\omega} \quad (6)$$

,where S12 is the transfer response of the network under consideration, and $S12_{min}$ and $S12_{AP}$ are its minimum-phase and all-pass components, respectively, such that $S12 = S12_{min} * S12_{AP}$. Equation 9 follows from the unity magnitude property of the all-pass component, while Equation 10 is obtained using the Hilbert transform for minimum phase systems. The methodology described in this paper uses the delay thus extracted to obtain causal signal flow graph equations for transient simulation of passive networks.

Signal flow graphs (SFGs) have been previously used in the transient simulation of passive systems [9]. One of the key advantages they provide is that it is possible to perform transient simulation without any kind of approximation/interpolation of the frequency response data. The signal flow graph of Figure 8 results

in a system of equations which need to be solved in order to generate the transient response of the circuit. These equations are given as

$$V_1(t) = V_S(t) + V_3(t) \otimes \Gamma_S \quad (7)$$

$$V_2(t) = V_1(t) \quad (8)$$

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t) \otimes s12(t) \quad (9)$$

$$V_4(t) = V_2(t) \otimes s21(t) + V_5(t) \otimes s22(t) \quad (10)$$

$$V_5(t) = V_4(t) \otimes \Gamma_L \quad (11)$$

Now, if the port-to-port delays of the system are known via the extraction process described above, Equations 9 and 10 can be re-written as

$$V_3(t) = V_2(t) \otimes s11(t) + V_5(t - Td) \otimes s_{min}12(t) \quad (12)$$

$$V_4(t) = V_2(t - Td) \otimes s_{min}21(t) + V_5(t) \otimes s22(t) \quad (13)$$

This new system of equations explicitly enforces the delay and the resulting solution enforces causality on the transient simulation.

One of the disadvantages of the SFG approach is that convolution needs to be performed at each time step. Since convolution is a computationally expensive procedure, requiring $O(N^2)$ operations, it reduces the simulation efficiency of the proposed methodology. One solution to this problem is the implementation of a fast convolution technique that is described in detail in [10]. Convolution performed using this technique requires *O(NlogN)* operations. Fast convolution considerably reduces the simulation time of the methodology proposed in this paper.

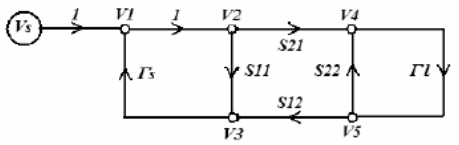
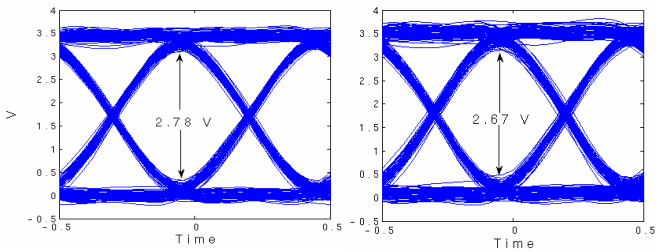


Figure 8. A sample signal flow graph

6. RESULTS

The methodology proposed in this paper was tested to perform SI-PI analysis on a number of systems that represent SiP solutions. A 64-bit interconnect bus referenced to non-ideal power/ground planes was simulated using random bit pattern excitations on each of the lines. The system output was observed in terms of an eye-pattern obtained on one of the lines. The PDN of the system was modeled using NAM to give a 128 port admittance matrix. The SDN was modeled using the Advanced Design System (ADS) from Agilent. This SDN was then integrated with the PDN using the stamp rule, and the consolidated system admittance matrix was reduced to give a 130-port response. Using the SFG based simulation approach, this system was simulated to obtain the required eye-pattern. The results are shown in Figure 9a.



(a) (b)

Figure 9. (a) Causal and (b) Non-Causal 64-bit bus simulation

To demonstrate the effects of causality violations on the signal integrity analysis of a system, the above system was re-simulated without delay extraction and causality enforcement. The results are shown in Figure 9b. It can clearly be seen that causality violations result in an artificial eye-closure; in this case of about 110 mV. In the future, as system rise time increases, this problem is expected to worsen.

7. CONCLUSION

The transition of future systems towards integration and miniaturization based on SiP has given rise to new SI and PI problems at the system level that include fringing fields, gap discontinuities and causality violations. This paper proposes a system level SI-PI analysis methodology and briefly describes the techniques that have been developed to address these problems. The proposed methodology has been successfully tested on a variety of test-cases including EBG structures, chip packages, etc.

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