Self-Calibration Technique for Reduction of Hold Failures in Low-Power Nano-scaled SRAM

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ABSTRACT
Increasing source voltage (Source-Biasing) is an efficient technique for reducing gate and sub-threshold leakage of SRAM arrays. However, due to process variation, a higher source voltage can significantly increase data flipping in standby mode (Hold Failures) resulting in faulty memories. This imposes serious concerns in reducing standby power with source-bias. In this paper, we analyze the effect of source bias on hold failures under both inter-die and intra-die variations. We propose a self-calibrating SRAM for aggressively reducing leakage while maintaining the hold failures under control.

Categories and Subject Descriptors
B.3.1 [**Semiconductor memories**]: Static memory (SRAM)

General Terms
Algorithms, Design, Experimentation

Keywords
Adaptive source biasing, hold failures, low power SRAM

1. INTRODUCTION
Aggressive scaling of CMOS devices in each technology generation has resulted in higher integration density and performance. As the integration density of transistors increases, leakage power becomes a concern in low-end mobile system-on-chips (SoC's) where the low standby power is crucial. Since today's processors and SoC's are mainly dominated by memory arrays, increased power of memory arrays adversely affects the power consumption and overall yield.

In nanometer scaled memory cells, most of the power is dissipated as leakage [1]. Many techniques, e.g., source biasing, body biasing, supply voltage scaling, have been proposed in past to suppress the leakage power in SRAM designs [2, 3, 4]. Among them, source-biasing technique is promising. Fig. 1(a) shows a typical source-biasing scheme for SRAM's. When a particular row is accessed, the source line (V_{SL}) is biased to zero which increases the drive current and achieves fast read/write operation. When the row is not accessed, V_{SL} is raised, which substantially reduces the both the sub-threshold and gate leakage during the inactive periods [4].

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Although increasing the source-bias voltage (V_{SB}) of source-line in SRAM array reduces the leakage power but the probability of retaining the data at the standby mode decreases (Hold failure). The principal reason of hold-failure in SRAM cell is the intra-die variation in threshold voltage (due to random fluctuation of dopant atoms) which causes mismatch in the strengths of different transistors in an SRAM cell [5-7]. Moreover, die-to-die variation in process parameters (say, V_t) has a strong impact on memory leakage. A memory with very low V_t transistors can have unacceptable amount of leakage. Since source biasing can be effectively used to reduce leakage, it is important to determine an upper bound of V_{SB} which can also preserve the correct data.

We have investigated the effects of source-bias on memory failure under variation to reduce leakage while maintaining its robustness. The contributions are summarized as follows:

- We study the effect of source biasing on both standby power and hold-failures of SRAM arrays.
- We propose an Adaptive Source-Biasing (ASB) scheme to minimize the leakage while controlling the hold failures.
- Finally, we suggest an on-chip self-calibration scheme for adaptive source-biasing of SRAM array.

The proposed self-calibrating SRAM with ASB scheme is simulated in predictive 70nm technology [8]. Simulation results shows that, adaptive source-biasing can result in 7-25% reduction in number of chips failing to meet leakage bound from zero source biased SRAM. Simultaneously, with ASB number chips failing in hold mode reduced by 7-85% from SRAM with fixed (optimum at nominal V_t corner) source biasing.

The paper is organized as follows. In Section 2, we discuss different sources of variations. In Section 3 and 4, we present the effect of source biasing on standby power and hold failures under inter- and intra-die process variations. In Section 5, we present an ASB condition for reliable SRAM operation in standby mode. We also propose a new on-chip self-calibration scheme to design low-power SRAM. Finally, we conclude the paper in Section 6.

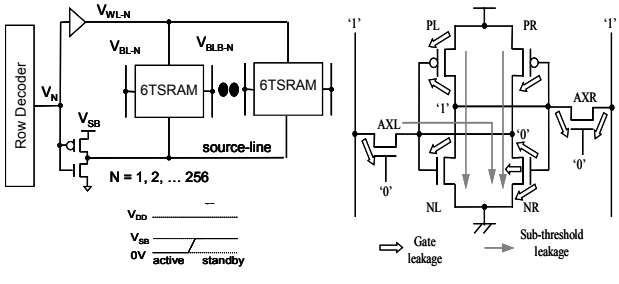


Fig. 1 (a) Structure of the source-biasing SRAM, (b) Dominant leakage components in a 6T SRAM cell

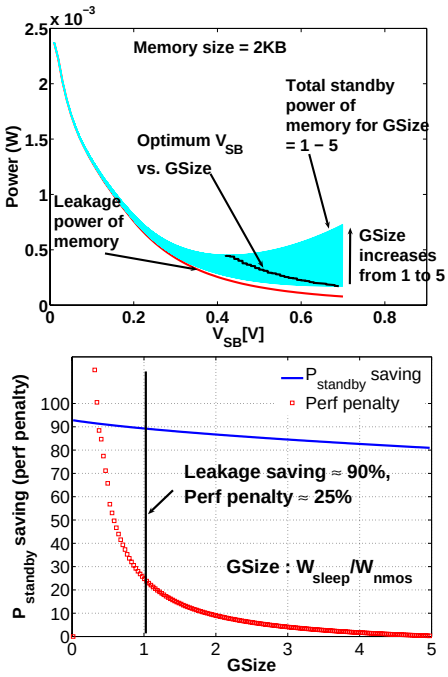


Fig. 2 (a) Standby power vs. source bias for variable GSize; and, (b) performance penalty and power saving vs. width of sleep transistor

2. SOURCES OF PROCESS VARIATION

Variations in transistor parameters e.g., channel length (L), width (W), oxide thickness (T_{ox}), etc. result in die-to-die and within-die variation in threshold voltage of a device. In this work, we considered both inter-die (ΔVt_{inter}) and intra-die (ΔVt_{intra}) variation in threshold voltage. ΔVt_{inter} has been modeled as a Gaussian distribution. Ideally, all transistors in a single chip should have same threshold voltages. However, random placement of dopant atoms in the channel, called random dopant fluctuation (RDF) [4] can give rise to threshold voltage mismatch between the transistors on a single chip. The impacts of RDF are most pronounced in minimum-geometry transistors commonly used in area-constrained circuits such as SRAM cells [7]. This can result in the threshold voltage mismatch (ΔVt_{intra}) between the neighboring transistors in a cell, resulting in parametric failures [14]. To estimate parametric failures, we have modeled ΔVt_{intra} of the transistors in SRAM cell as six independent Gaussian random variables. Predictive 70nm devices [8] were used for circuit simulations in Hspice.

3. STANDBY POWER REDUCTION USING SOURCE BIAS

The leakage of an SRAM cell is due to sub-threshold, gate and junction tunneling leakage as shown in Fig. 1(b) [7]. In standby mode, leakage of an SRAM cell can be reduced by raising the voltage of the "source-line" to a positive value (V_{SB}). This increases the node storing "0" from 0V to V_{SB} resulting in a negative V_{gs} (and negative V_{bs}) operation of access transistor AXL, thereby, reducing its sub-threshold leakage. NMOS transistor NR has a lower V_{ds} and a negative V_{bs} which also reduces its sub-threshold leakage. Leakage of PMOS transistor PL is reduced due to lower V_{ds}. Moreover, raising the source bias reduces the rail-to-rail bias across the cell, thereby reducing its

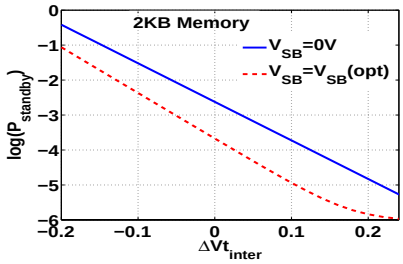


Fig. 3 Standby power for V_{SB} = 0V and V_{SB} = V_{SB}(opt)

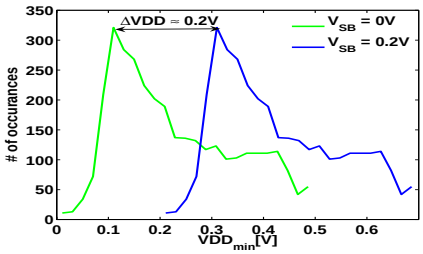


Fig. 4 Distribution of the data retention voltage (V_{DDmin}) for different source-bias voltage

gate leakage. Therefore, substantial leakage savings can be obtained by controlling the source line voltage (source of NL and NR) [4].

3.1 Leakage variation due to process fluctuations

The random inter- and intra-die variation in threshold voltage results in significant variation in cell leakage, particularly, the sub-threshold leakage. Since, sub-threshold leakage depends exponentially on V_t, the leakage distributions of different SRAM cell can be considered as independent log-normal variables [7, 14]. Although the intra-die process variation increases the leakage spread (standard deviation/mean) of a single SRAM cell, the overall spread of the memory array leakage (which is summation of a leakage of a large number of cells) is low [14]. Hence, the leakage distribution due to intra-die variation of an SRAM array can be well-characterized by its mean value only. Therefore in this work, we have considered only the mean value of array leakage due to intra-die variation. However, inter-die variation in V_t results in a large spread in the mean leakage of an array. This can cause some of the SRAM dies to have a very high leakage (more than tolerable limit). These dies, violating the power budget should be discarded resulting in a yield loss due to leakage. Based on the above discussion we define "leakage yield" as:

$$Leakage\ Yield = \frac{\#of\ dies\ with\ L_{MEM}\left(=\sum I_{cell}(\mu_{cell})\right) < L_{MAX}}{total\ \#\ of\ dies} \quad (1)$$

3.2 Optimization of Source Bias under performance constraint

Source-biasing can significantly reduce leakage of an SRAM array. However, it increases the other components of standby power e.g., leakage power of sleep transistor and transition energy dissipated while switching between sleep mode and normal mode. The total standby power of a source-biased SRAM cell is given by

$$P_{total} = P_{cell} + P_{sleep} + P_{switching} \quad (2)$$

where P_{cell} is the leakage power of a single cell (mainly sub-threshold), P_{sleep} is the leakage power of the sleep transistor (Fig.

1) and $P_{transition}$ is the transition power due to activity in sleep transistor. Assuming the device leakage is dominated by the sub-threshold leakage, we obtain:

$$P_{cell}(V_{SB}) \sim P_{cell}(0)\exp(-qV_{SB}/mkT)$$
$$P_{sleep}(V_{SB}) \sim V_{SB} \times W_{sleep} I_0 \exp(-q\lambda_D(V_{DD}-V_{SB})/mkT) \quad (3)$$
$$P_{switching}(V_{SB}) \sim \alpha f\left[(W_{sleep}+2*W_{nmos})C_{drain}+C_{INT}\right]V_{SB}^2$$

where, I_0 is the current of an 1µm NMOS at V_{gs}=0, V_{ds}=V_{DD} and V_{bs}=0, '*m*' is the sub-threshold swing factor, λ_D is the DIBL coefficient, C_{drain} is the drain capacitance of an NMOS, C_{INT} is the interconnect capacitance connected to "source-line", α is the transition activity (~1%) and *f* is the frequency of operation. If the total number of cells in SRAM array is N_{cell}, then the total standby power ($P_{standby}$) is given by $N_{cell}P_{total}$. From equation (3), it is evident that increasing V_{SB} reduces the array leakage exponentially, but increases the sleep transistor leakage and transition energy. Similarly, a higher sleep transistor width tends to reduce leakage saving due to higher transition energy and larger sleep transistor leakage. Hence, for a certain W_{sleep} there exists an optimum value of V_{SB} which minimizes the overall standby power ($P_{standby}$). Fig. 2(a) shows the total standby power of a 2KB memory array with source biasing for different sizes of sleep transistor in nominal process corner. From this figure, it can be noted that (a) total standby power reduces rapidly with V_{SB} due to reduction in memory leakage but at high V_{SB}'s, the power increases due to high transition energy consumption; and, (b) the leakage and transition energy of sleep transistor increases with GSize (=W_{sleep}/W_{nmos}) at high V_{SB} corners. Therefore, for each GSize we get a corresponding value of V_{SB} where maximum power saving can be attained (Fig. 2(a)).

It is evident from equation (3) that a small sleep transistor improves leakage saving. However, it also increases the access time during normal read operation. Therefore, a trade-off is required to select reasonable size of sleep transistor to minimize power under a performance constraint. In Fig. 2(b), we plot the saving in standby power and performance penalty with GSize. It can be observed that 90% standby power can be saved at the cost of 25% performance penalty (at nominal process corner) when GSize is 1. The corresponding optimum value of V_{SB} (called $V_{SB}(opt)$) is found to be 0.63V.

Fig. 3 shows the standby power for a 2KB memory array estimated using equation (2) with inter-die variation for zero and optimum source-biases (i.e., V_{SB}(opt)). It indicates that source biasing plays an effective role in reducing the standby power at low V_t corners. However at extreme high V_t, the impact of source biasing reduces because the leakage is already small and the leakage saving is masked by the transition energy overhead associated with the switching of sleep transistor.

4. IMPACT OF SOURCE BIAS ON HOLD FAILURE

In this section, we will study how the source bias affects the hold failure probability of the memory under process variation.

4.1 Hold failure

A lower rail-to-rail bias (V_{DDH}) at the standby mode in a source-bias SRAM reduces the node storing "1" from the applied V_{DDH} (in other words, node storing "0" is higher than V_{SB}). This is due to the leakage of the NMOS transistor. If the voltage at node storing "1" becomes less than the trip-point of the inverter associated with node storing "0", the cell flips in the hold mode. The principal reason for hold failure in SRAM cell is the intra-die variation in threshold voltage due to random fluctuation of dopant atoms [6, 7]. The intra-die process variation results in fluctuations in the minimum V_{DD} at which the data can be retained (i.e. V_{DDmin}). The hold failure probability (P_{HF}) due to this spread in V_{DDmin} for a source-bias cell is given by:

$$P_{HF} = P(V_{DD\min} > (V_{DD} - V_{SB})) \quad (4)$$

A column is said to be faulty in hold mode, if any of the cell in that column fails due to data retention violation. If the number of faulty column is larger than the number of redundant column, the array fails. Using the method proposed in [7] we can estimate hold failure probability for an SRAM array (P_{HF}(memory)). The hold failure in standby mode can degrade the memory yield [7]. However, the variation in inter-die V_t can increase hold failures.

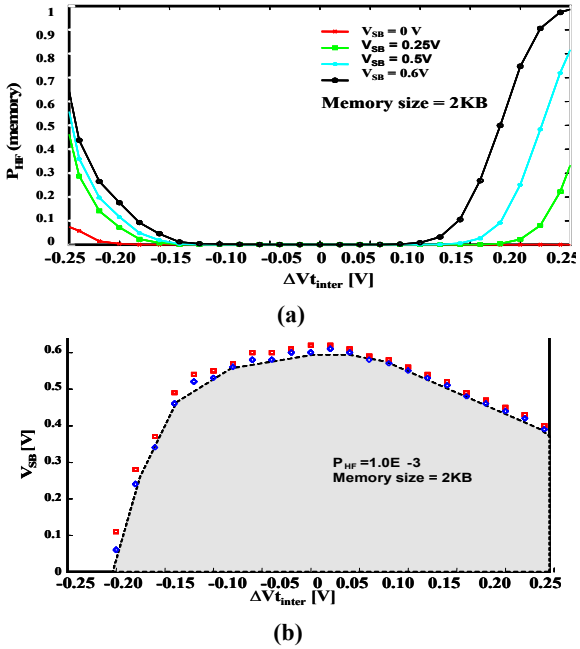


Fig. 5 (a) Hold failure probability with inter-die variation under different source-biasing; (b) source biasing voltage for a target hold failure probability under inter-die variation

4.2 Effect of source bias on P_{HF}

Fig. 4 shows the distribution of V_{DDmin} with inter-die process variation for two V_{SB}'s. A higher V_{SB} requires a higher V_{DDmin} to hold the data (i.e. V_{DDmin} distribution shifts towards a higher value). Fig. 5(a) shows the hold-failure probability of a 2KB memory array at different inter-die corner and V_{SB} (calculated using V_{DDmin} distributions at different V_{SB} and ΔVt_{inter} and (4)). It shows that a negative shift in the threshold voltage due to inter-die variation, (i.e. for the SRAM arrays shifted to the low-V_t process corners) increases the hold failure. This is because of the fact that negative V_t shift increases the leakage through the transistor N_L, thereby, increasing the hold failures. The hold failure also increases at the high V_t corners, as the trip-point of the inverter PR-NR increases with positive V_t shift. Hence, the overall memory failure due to hold violation increases both at low

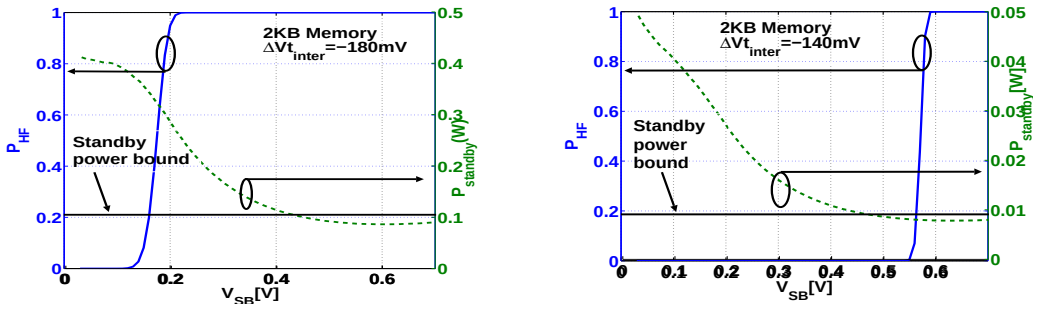


Fig. 6 Hold-failure probability and standby power with source biasing voltages at (a) ΔVt_{inter}=-180mV (b) ΔVt_{inter}=-140mV

and high-V_t corners. However, the hold failure probability of the array remains minimum at the nominal V_t corner.

It is interesting to note that as the V_{SB} increases, the hold failure probability increases for a high inter-die V_t corner. This is due to the fact that a higher V_{SB} increases the voltage at the node storing "0" and therefore, weakens the node storing "1" (weaker PMOS). This is further enhanced by the higher trip-point (due to higher V_t of the devices) of the inverter associated with the node storing '0'. Hence it can be more easily flipped. At low V_t corners, a higher leakage of the NMOS increases hold failures. A higher V_{SB} tends to reduce the leakage current. However, it also reduces the rail-to-rail supply (which has a stronger impact compared to leakage), thereby increasing the hold failures. Hence, the for a target hold failure probability, V_{SB} cannot be increased too much at both high and low inter-die Vt corners (Fig. 5b). However, a higher V_{SB} can be safely used for the chips at nominal corner.

5. ADAPTIVE SOURCE BIASING FOR RELIABLE SRAM

From the results of Section 4, it can be concluded that a fixed V_{SB} may not be used across all the chips to meet a target hold-failure probability. In general, V_{SB} must be increased to reduce the standby power as much as possible. However, the maximum V_{SB} at an inter-die corner is ultimately limited by the hold failures. For example, consider a 2KB memory array chip lying at ΔVt_{inter} = -180mV (Fig. 6 (a)). As it can be observed from this plot, a maximum of 100mV source biasing can be applied without causing hold failures. However, the standby power cannot be reduced to meet the target standby power bound (assumed 10 times larger than standby power at nominal corner) with this amount of V_{SB}. Therefore these chips will contribute towards yield loss due to excessive standby power. However, for the chip at ΔVt_{inter} = -140mV (Fig. 6 (b)), the V_{SB} can be increased till 550mV safely. The standby power also meets the target bound under this V_{SB}.

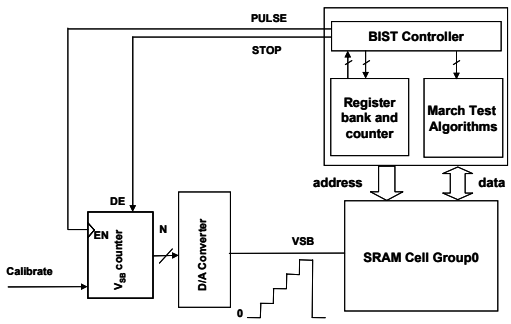


Fig. 7 Automatic self-calibration scheme for adaptive source-biasing

5.1 Self-calibration procedure

From the examples discussed above, it is obvious that the source voltage can be adaptively tuned at each process corner to reduce the standby power while maintaining the target number of hold failures. The target number of hold failures, in turn, depends on the number of available redundant columns for repairing purposes (assuming that only column redundancy is present in the system). Given *NRC* number of redundant columns, V_{SB} can be increased till all the redundant columns have been exhausted for repairing the faulty columns (due to hold failures). Fig. 7 shows the block diagram of a self-calibration system for adaptive source biasing. In an initial calibration cycle, it determines the value of source bias and subsequently uses this value during standby mode of the memory. The self-calibration system consists of a Built-in Self-Test (BIST) circuit to perform read and write operations on the memory array. The source bias is generated by converting a digital counter value to an analog voltage. The counter value is incremented by the BIST controller. The BIST maintains a register bank of size 1xNC (where NC is the number of columns in the memory array) to store the faulty column information. Each register corresponds to an entire column. The register bit is set to '1' if a fault is detected in any row of that column. Another counter (inside the BIST) keeps track of the total number of registers with value '1'. The counter value indicates the number of faulty columns in the array. The counter value greater than NRC for a particular V_{SB}, indicate that all redundant columns have been used. Therefore, the present V_{SB} can be considered as adaptive source bias value, V_{SB}(adaptive). The operation of BIST for adaptive calibration of source bias is more clearly understood from Fig. 8. A simple MATS [13] algorithm is used to determine the hold failures at different V_{SB}'s. Note that, performing March test and switching between active and standby mode to determine the hold failures may take long test time during initial calibration. To reduce the calibration time, we propose to divide the entire SRAM array into several sub-blocks and determine the V_{SB}(adaptive) of each sub-blocks in parallel.

In our simulation to determine the adaptive source biasing voltage for a 2KB memory array, we pick a chip from an inter-die corner and find the total number of failing cells (N_F) at a source bias

$$N_F = N_{cells} P_{hfcell} \quad (5)$$

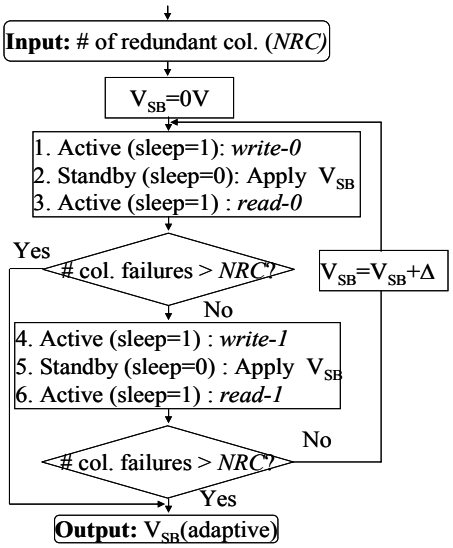
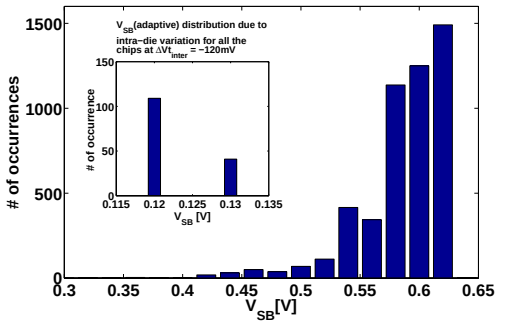
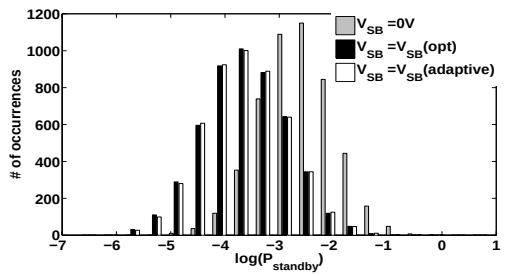


Fig. 8 Flowchart for determination of V_{SB}(adaptive)

where N_{cells} is the total number of cells present in the memory array and P_{hfcell} is the hold failure probability of single cell. Since, these failures have equal probability of happening at any memory location, we randomly distribute the faulty cells in the memory array. Next the total number of failing columns are also determined and compared against NRC. If the number of faulty columns is less than NRC, we increase the source bias and perform the test again. We continue this process until the number of faulty columns exceeds NRC. Note that we also consider failures in the redundant columns in our simulations. Fig. 9(a) shows the source bias voltage (called V_{SB}(adaptive)) found at different inter-die corner (between -200mV < V_{SB} < 200mV) by following this methodology. We assumed 5% redundancy in our simulations. It can be observed from this plot that the range of



(a)



(b)

Fig. 10 (a) Distribution of Source-Bias in ASB (b) Distribution of standby power with zero V_{SB}, V_{SB}(opt) and V_{SB}(adaptive)

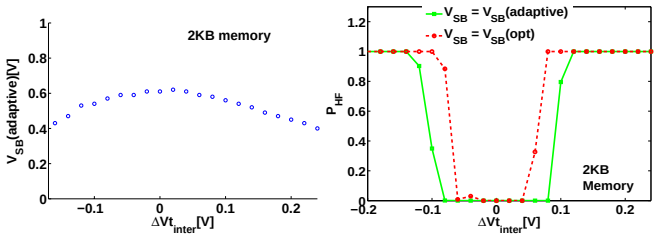


Fig. 9 (a) Adaptive source-biasing voltage for different inter-die corners (VSB(opt)=0.63), (b) hold failure probability with inter-die variation for V_{SB}(opt) and V_{SB}(adaptive)

V_{SB}(adaptive) is 0.40~0.60V. For the nominal corner, (i.e., ΔVt_{inter} = 0mV), V_{SB}(adaptive) is 0.60V. This figure clearly illustrates the need of adapting V_{SB} according to the process corner.

To understand the effectiveness of the proposed Adaptive Source Biasing (ASB) scheme, we estimated the hold failure probability of the SRAM array (considering redundancy, as explained above) at different inter-die corner. In the absence of the ASB scheme, we could apply V_{SB}(opt) (which is determined at nominal corner considering standby power and performance) to all the SRAM dies. However, it can be observed from Fig. 9(b), application of V_{SB}(opt) will increase the number of dies failing in hold-mode (the window of low hold failure is narrow). This is due to the fact that, at low and high inter-die V_t corners, 'hold' failures are more probable [14]. On the other hand, if an ASB scheme is used, the proposed system modifies the applied source bias based on the inter-die process shift. This reduces the number of hold-failures at low and high-V_t inter-die corners (Fig. 5b). Hence, adaptive source biasing widens the low memory failure (hold) probability window, which helps improve SRAM yield under variation

5.2 Statistical simulation results

It is observed in Fig. 9(b) that adaptive source biasing can reduce the number of SRAM dies failing in hold mode. To fully evaluate the effectiveness of the proposed technique we performed a statistical simulation using predictive 70nm devices, considering both inter-die and intra-die process (V_t) variation. First we generated 5000 inter-die V_t points following a Normal distribution. Next we estimated the proper source bias required at each inter-die corners. The application of adaptive source biasing results in a distribution of the source bias applied to different dies as shown in Fig. 10 (a). It should be noted that, during a statistical simulation, there can exist a finite number of dies with a particular inter-die V_t shift. For all the dies, the proper source bias can be different. This is because, the hold failures in an array not only depends on 'number of faulty cells' but also on 'location of the faulty cells'. For example, if an array has 2 redundant columns and 3 faulty cells, it is possible that all the faults happen in the same column. Under this condition the array is repairable and don't count towards yield loss due to hold failures. However, if the 3 faults appear in 3 different columns we will get an SRAM die failing in hold mode. This example shows that, there is a possibility that, for several dies at a particular inter-die V_t shift, the proper source bias is different. It is shown in Fig. 10(a) that, for a same inter-die corner we might get two different proper source bias values. However, this effect is expected to be very small as a new fault has a higher probability of being in a different column. Hence, we observed that this effect does not strongly impact source bias distribution.

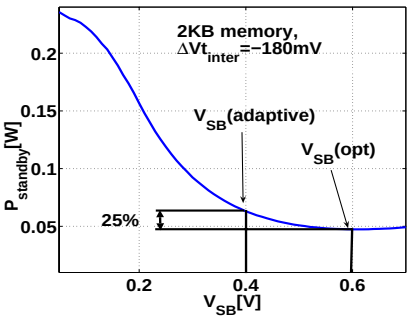


Fig. 11 Change in standby power between VSB(opt) and VSB(adaptive)

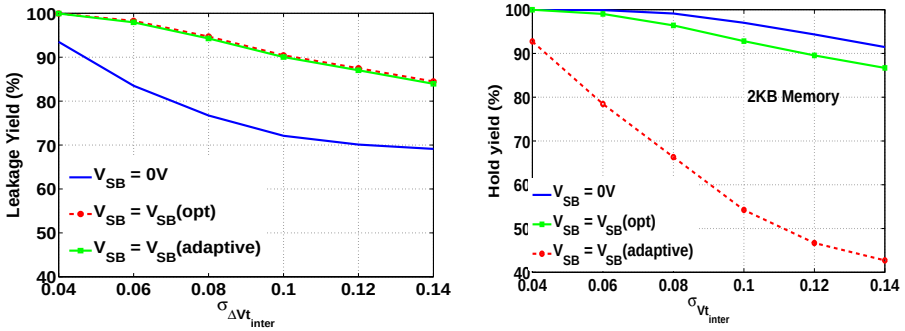


Fig. 12 (a) 'Leakage yield' with zero V_{SB}, V_{SB}(opt) and V_{SB}(adaptive) for different standard deviation of ΔVt_{inter}; (b)'hold yield' with zero V_{SB}, V_{SB}(opt) and V_{SB}(adaptive) for different standard deviation of ΔVt_{inter}

Finally, we estimated the leakage (mean) of the SRAM dies at different inter-die V_t corners (Fig. 10(b)). It can be observed that, both V_{SB}(opt) and adaptive source bias shifts the leakage distribution towards lower values (i.e. towards left in Fig. 10(b)). This suggests that, application of V_{SB}(opt) and adaptive source bias improves leakage yield (i.e. number of dies meeting the leakage/stand-by power bound). It should be further noted that, the adaptive source bias does not strongly modify the leakage distribution from V_{SB}(opt). Particularly in low-and high inter-die V_t corners, value of the selected source bias in an ASB scheme, is lower than V_{SB}(opt). Hence, it is expected that, array leakage will be higher in case of adaptive source bias. However, it should be noted from Fig. 9(a) that, reduction in adaptive source bias value from V_{SB}(opt) is not very high, even at low or high inter-die V_t corners. Moreover, a reduction in source bias reduces both the transition energy (comparable to array leakage at high-V_t corner as leakage is very low) and the sleep transistor leakage (non-negligible at low- inter-die V_t corner). Hence, the change in total standby power from V_{SB}(opt) to adaptive source bias is small. This is further clarified in Fig. 11, which shows that, the change in total stand-by power for a low-V_t die from V_{SB}(opt) (~0.6V) to adaptive source bias value at that corner (~0.4V) is only ~25%. This explains the negligible difference between the leakage distribution between V_{SB}(opt) and adaptive source bias cases. Negligible difference between the two distributions suggests that, there is a only a very small yield loss in ASB scheme (due to high stand-by power) compared to V_{SB}(opt). Fig. 12(a) shows the variation in 'leakage yield' with an increase in inter-die process variation. It can be observed that, both V_{SB}(opt) and adaptive source bias significantly improve leakage yield compared to conventional zero source bias design. However, the difference between the 'leakage yield' due to V_{SB}(opt) and adaptive source bias is minimal. It suggests that, adaptive source bias does not degrade leakage yield. On the other hand, adaptive source biasing has much better 'hold yield' compared to V_{SB}(opt) (Fig. 12(c)). The proposed self-calibrating SRAM with ASB scheme is simulated in predictive 70nm technology [8]. Simulation results shows that, adaptive source-biasing can result in 7-25% reduction in number of chips failing to meet leakage bound compared to zero source biased SRAM. Simultaneously, with ASB number chips failing in hold mode reduced by 7-85% compared to SRAM with fixed (optimum at nominal V_t corner) source biasing. Hence, the statistical simulation of the ASB scheme shows that the proposed system can achieve better robustness without increasing power dissipation.

6. CONCLUSION

Technology scaling significant increases the leakage power and degrades parametric yield of SRAM. In this paper, we investigated the impact of a standard leakage reduction technique, namely *source biasing* on hold failures of SRAM arrays. Our analysis shows that, conventional source-biasing can negatively impact parametric yield by increasing hold failures. Hence, there is a strong need for design techniques that can reduce leakage power in SRAM without degrading the parametric failures. We proposed a self-calibrating SRAM which can significantly reduce leakage spread, while maintaining hold failures under control. Simulation result in predictive 70nm technology shows 7-25% improvement in leakage yield compared to conventional SRAM. Simultaneously, 7-85% reduction in yield loss due to hold failure is observed compared to standard source-bias SRAM. Hence, we believe that the proposed self-calibrating SRAM can reduce standby power without significant yield degradation.

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7. REFERENCES

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