The Importance of Adopting a Package-Aware Chip Design Flow

Kaushik Sheth
Rio Design Automation
2901 Tasman Drive, Ste 112
Santa Clara, CA 95054-1137
+1-408-844-8038 x11
ksheth@rio-da.com

Egino Sarto
Rio Design Automation
2901 Tasman Drive, Ste 112
Santa Clara, CA 95054-1137
+1-408-844-8038 x 14
sarto@rio-da.com

Joel McGrath
Rio Design Automation
2901 Tasman Drive, Ste 112
Santa Clara, CA 95054-1137
+1-408-844-8038 x 15
jmcgrath@rio-da.com

Abstract
In this paper, we talk about the short- and long-term implications of ignoring the relationship between the chip, package and PCB during I/O planning and how these issues will manifest themselves as we move toward 65 and 45nm technology.

It also introduces a whole new approach to chip/package I/O planning and optimization. This new approach simultaneously synthesizes the entire interconnect from the I/O driver to the package ball and establishes an interconnect plan that is optimized for both chip and package.

Categories and Subject Descriptors
J.6 [**Computer-Aided Engineering**]: Computer-Aided Design

General Terms: Algorithms, Design, Experimentation, Standardization, Verification

Keywords: Co-Design, Chip, Package, Substrate, I/O, Synthesis, Prototyping, Exploration, RDL, Concurrent, Flip Chip, Routing,

1. Introduction
Many chip designers assume that the package is the package designer's problem, when in fact, the impact the package has on chip performance is a system-level problem with few automated solutions. Many chip designers rely on spreadsheets for I/O planning and chip to package net mapping decisions. With package performance, complexity and cost having a greater impact for the chip designers, a new approach to integrated circuit (IC) design that is package and system aware is required.

Floorplanning of the chip and placement of I/Os cannot be done in isolation and a comprehensive approach that allows a concurrent design methodology for chip and package is a must. Package-aware I/O planning is essential for meeting cost, time-to-market and performance targets. Without this planning, package complexity can increase product cost, often pushing a chip's package cost higher than the cost of its silicon. I/O problems also may limit performance and go undetected until verification; the numerous design cycles required to correct the problems may delay time to market by weeks. Even without these problems, the traditional I/O design methodology adds weeks to the system on chip (SoC) design schedule.

DAC 2006, July 24–28, 2006, San Francisco, California, USA.

2. Holistic Design Approach
What's needed is a new approach to the way these challenges are addressed that adds "interconnect synthesis" into the flow. Interconnect synthesis is a process in which cross domain interconnect — chip/package and PCB — is taken as a whole into consideration during I/O planning and sequencing. Package-aware I/O planning is especially critical for flip-chip implementations and includes I/O synthesis, placement and routing. I/O synthesis creates an optimized I/O plan combined with cost-effective packaging options, while satisfying physical and electrical constraints.

This holistic approach to chip design, including the impact of the package parasitics on the interconnect performance, ensures that all elements are taken into consideration as part of the optimization process. (see Figure 1)

It should be able to accept various constraints from diverse design domains including printed circuit board (PCB), package and IC. It should be able to produce optimal placement of I/Os, associated logic, bumps and routing on the top layer from I/Os to bumps. A capability is needed to synthesize the bump patterns to achieve timing closure, signal integrity requirements, and escape in the given package substrate layers along with exploration capabilities. Developing such a solution for full chip integration early in the design and being able to simultaneously visualize the chip in the package ensures design convergence. It would help chip designers iteration-free verification when the design is done and eliminate the ad-hoc approach to chip-package design.

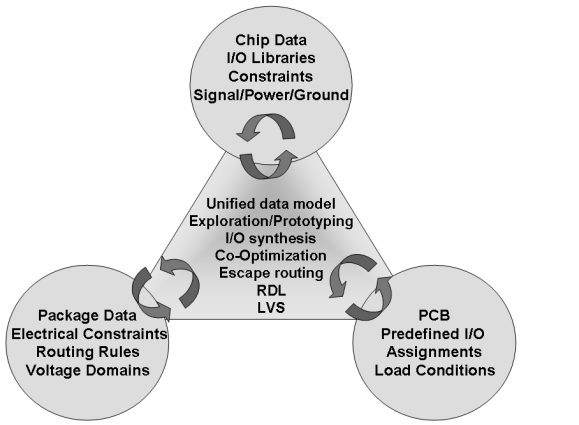


Figure 1. Holistic view co-optimization

3. System Design Flow

The most important I/O planning concept is that I/O planning must be part of the overall system design flow. Chip designers need not become packaging experts; packaging guidance can be built into design tools. They do need to understand some packaging concepts that have long been ignored. By introducing automated I/O planning early in the design cycle, SoC project managers can ensure good I/O performance for signal integrity, power integrity, physical implementation and lowest overall cost.

Chip designers are often surprised by the complexity of SoC packages. A typical 2,000 ball SoC package can have up to 12 layers containing an intricate escape pattern of interconnects and vias. Unlike silicon design rules, package design rules are flexible, but come at a cost. The package designer can decrease the interconnect pitch to fit more routes in congested areas, but the finer pitch tends to reduce manufacturing yields and increase package cost. The finer pitch may also cause signal integrity problems. The package designer has other options, including increasing the number of layers, but each additional layer increases the package cost.

Package design is a manual process because it involves many layout, cost and performance judgments rather than fixed routing rules. As a result, skilled package designers can minimize costs and performance problems and accommodate the I/O layout done by the chip designer. However, even the most skilled package designer cannot overcome poor I/O planning at the chip level because chip designers rarely create I/O layouts with packaging in mind. This means finding a workable escape pattern is often a long process. For example, designing a typical eight-ten layer package can take between four and six weeks. (See Figure 2)

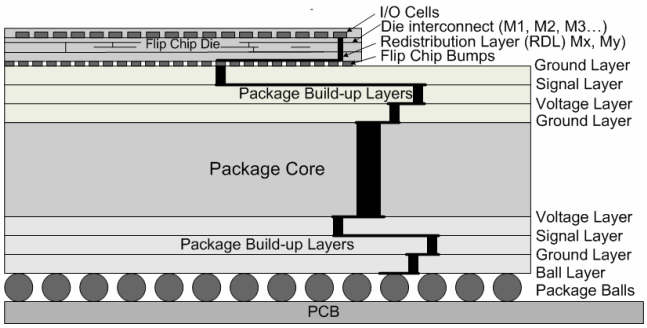


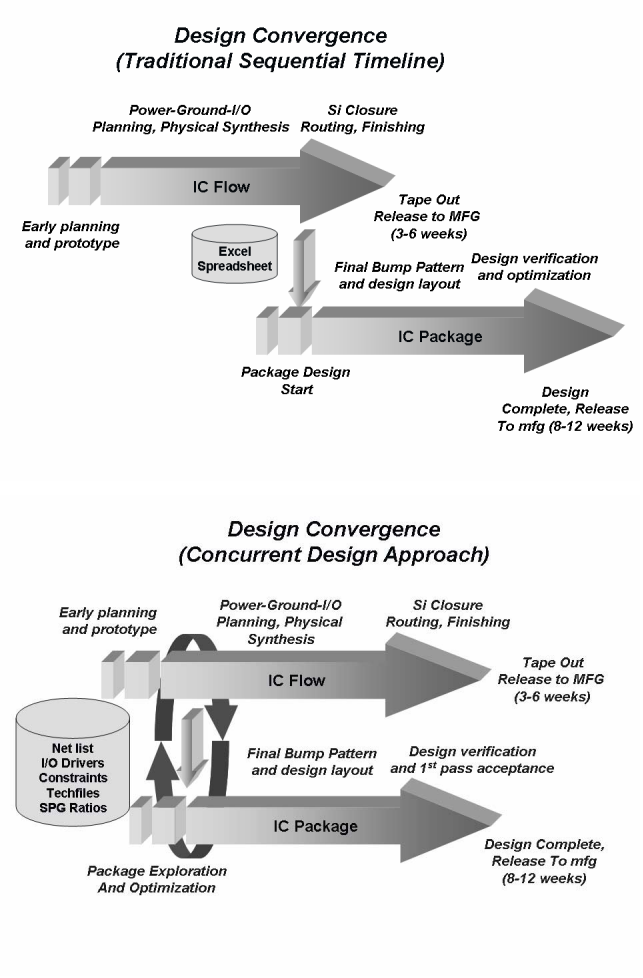
Figure 2, Flip Chip Interconnect Path

4. Ever Increasing I/O Counts

The growing number of SoC I/Os is guaranteed to increase package cost and design time. Signal integrity concerns have become more pressing as I/O speeds increase and voltage levels decrease. Further, the use of system-level packages (SLPs) that integrate one or more ICs with other components in a single compact package increases package design requirements.

Designing a digital SoC using a package-aware I/O plan begins with the estimated number of I/Os and a set of performance requirements. It determines the required number of power and ground nets for each voltage domain, the escape patterns and power delivery for flip-chip ICs, and the wire-bond pattern for wire-bonded chips.

With this information on the package I/O assignments, the package designer can create the initial package layout at the beginning of the silicon design flow. This updated design flow enables a radical departure from the traditional sequential design of chip and package to a concurrent design approach. (see Figures 3 and 4)



Figures 3 and 4, Traditional and Concurrent Design Flows

An early I/O and package plan lets designers analyze the entire interconnect, from the chip's I/O buffers to the PCB. The timing and signal integrity (SI) data provides a basis for defining the chip and package design constraints for designs that are routable. Package-aware I/O planning reduces costs by discovering the minimum die size possible via optimized I/O and bump placement combined with a cost-effective package option.

5. The March Toward 65 and 45nm

The impact of moving toward 65 and even 45nm design is that chips that were once core limited, are now becoming pad limited. The shrinking of the core combined with the increasing I/O counts means that upfront I/O planning is even more critical.

In the case of wire bond designs, stacking of I/O may be the only method available for reducing die size. However stacking wire bonded I/O results in more wires crossing which can lead to a significant increase in mutual inductance. Proper I/O sequencing

can help in minimizing inductance. To effectively determine the proper sequencing, I/O synthesis combined with SI analysis must be performed at the early stage of design so that the I/O plan can be established and the core designed accordingly.

In the case of flip chip designs, multiple rings and area I/O have proven to be effective methods for controlling die size. However these compact I/O plans drive package escape complexity to a much higher level. Even today, package escape routing of flip chip designs can have a major impact on schedule and cost. Packing even more I/O at tighter spacing will only exacerbate the problem.

To manage these high density designs, I/O synthesis must simultaneously consider the chip area available to place the I/O, RDL to make sure nets are routable on the chip, bump placement that adheres to package spacing rules, package escape routing that uses a minimal number of layers to control cost while all along honoring electrical constraints such as differential pairing, voltage domain separation and timing. (See Figure 5)

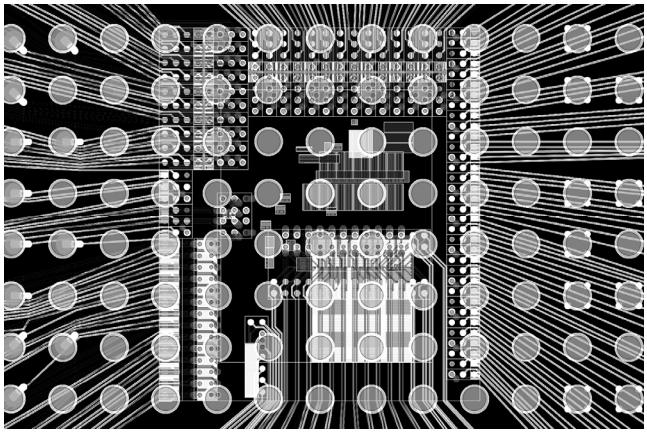


Figure 5, I/O Placement, RDL, Bump Placement, Package Escape Routing, Bump-Ball Assignment and Routing

Another phenomenon that designers are experiencing with these dense flip chips is coupling between the chip and the package. This can occur when the top layer of the package under the die is used for the routing of high speed nets. This is becoming more common with the use of area array.

6. Unified Data Model

For both chip and package I/O planning includes synthesis, placement and routing, and the ability to analyze timing, power and signal integrity for both chip and package. These functions must work with industry-standard data files — such as DEF and LEF — and tool interfaces. To enable simultaneous representation of the entire chip and package, the I/O planning environment needs a unified data model represented in a common database. Along with providing the basis for optimizing an initial I/O plan for the chip, it helps resolve I/O-related questions throughout the design flow. At any point in the flow, chip designers can interactively view the impact of I/O changes to the chip floorplan.

The methodology also requires a user interface for collecting and managing I/O data in an integrated bump BGA map. In contrast to the error-prone task of entering and maintaining I/O data in a general-purpose spreadsheet, the I/O planning interface acts as a dynamic repository with the correct state of the I/O plan.

7. Synthesis and Placement

Synthesis and placement create a correct-by-design I/O ring that satisfies a set of constraints, including signal/power/ground (SPG) requirements, package design rules, the core floorplan, and board-level I/O requirements. To meet the SPG requirements, synthesis must consider signal and power-integrity factors, including the power and ground needs of I/O drivers. Synthesis must calculate the current requirements of a particular voltage plane based on the driver models, and then calculate the number of balls needed to meet those current requirements. For designs that have multiple voltage domains, synthesis must accommodate the needs of each power domain.

While satisfying these constraints, the synthesis engine must optimize the I/O ring plan for minimum die size, core and I/O row area. If the die size is fixed, the synthesis algorithm can succeed only if a feasible I/O ring plan exists for the given die size. When feasible, the optimized plan maximizes the usable area for core placement.

The placement engine must place I/Os, bumps or bond pads, and assign nets to pins/balls Before synthesis, the engine estimates I/O cell placement around the periphery of the die. It is essential for this placement to accommodate requirements such as pre-placed instances and groupings of I/O cells along with electrical constraints. As with all I/O planning steps, algorithms must respect the special needs of differential pairs.

After the I/O ring is synthesized, the placement tool can generate a legal I/O placement. After creating the initial package routing, resistance, inductance and capacitance can be extracted for the nets and analyzed for I/O timing and noise, the router must extract resistance, inductance and capacitance (RLC) parasitics for the nets and analyze them for I/O timing and noise. Final detailed routing of the package is left to the package designer, who can apply manufacturing yield optimization techniques using specialized electronic design automation (EDA) software for package design.

8. Extraction and Simulation

I/O planning software needs a variety of analysis engines. Extraction/estimation is used to obtain initial parasitics information about the die and package nets. Final signoff accuracy requires use of a full 3D field solver, but early-stage analysis benefits from fast estimates of parasitics. In these early stages, PCB traces can be represented as distributed RLC circuits with standard terminations such as series resistors.

Using this and other data, delay engines can calculate timing effects due to resistance, capacitance, inductance, conductance and crosstalk. These engines must be able to calculate the delay associated with individual nets or groups of nets. Delay engines should also determine the timing skew for differential pairs, clock switches and data/clock nets.

A signal integrity engine supplies crosstalk data needed for delay analysis and noise estimation. Using extracted package parasitics and IBIS driver models, it helps optimize the I/O plan in synthesis. (see Figure 6) Similarly, a power integrity engine analyzes voltage and current values on power nets. A frequency-domain analysis is useful for determining de-coupling strategies. A time-domain

analysis looks at electrical characteristics and groups of signals based on their resistance, inductance, capacitance and mutual coupling. Together, the two types of integrity analysis can enable I/O planning software to optimize power/ground-to-signal ratios.

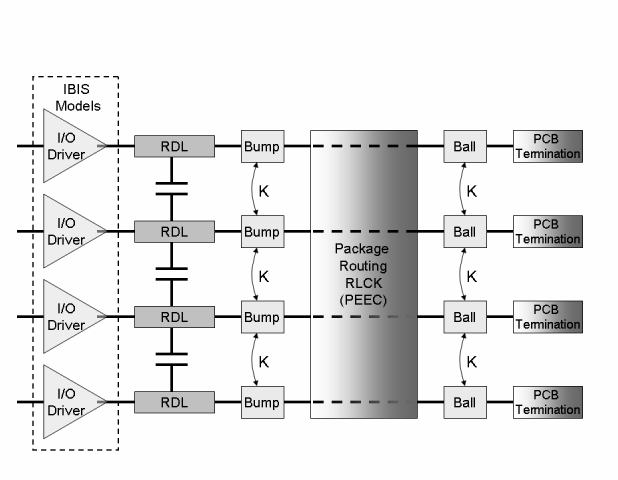


Figure 6, Driver to Bump to Package Ball Interconnect Analysis

With this data flow, I/O planning software can collect the disparate types of I/O data in use today and provide a path from chip to package designers.

9. Tool Interoperability

Tool interoperability among the leading EDA vendors is very limited. Even within the same vendor tool set, a total lack of any commonality with native databases makes cross domain analysis a difficult proposition. Each translation of data into some generic exchange format such as lef/def, ASCII, GDSII or DXF not only removes otherwise important content but makes what should be a simple process laborious and error prone.

Standards such as OpenAccess hold out the promise of greater interoperability, however adoption is slow and each supplier adds their own "uniqueness" to their implementation. In addition, OpenAccess, or any industry standard translation medium is non-existent in the IC Packaging or PCB domain.

10. Conclusion

Chip designers have ignored packaging and endured longer time to market, higher costs and compromised performance. With package-aware I/O planning for chip design, they can reduce costs through die size reduction, the use of less expensive package technology and reduced package complexity. The design cycle will be shorter due to concurrent chip and package design flows that simplify I/O management, helping beat time to market pressures. Chips will offer higher performance due to realistic design constraints and the ability to manage power and signal integrity and timing to PCB.

Additionally, package-aware I/O planning enables design groups to get early information about the type of packaging needed for a specific design, helping manage cost and schedule projections.

Ignoring the relationship between the chip, package and PCB is no longer an option for chip designers. What's needed is an effective means of bridging the gap between the design of high-performance chips and packages, and a chip's integration with the rest of the electronic system.