Energy-Scalable OFDM Transmitter Design and Control

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ABSTRACT
Orthogonal Frequency Division Multiplexing (OFDM) is the modulation of choice for broadband wireless communications. Unfortunately, it comes at the cost of a very low energy efficiency of the analog transmitter. Numerous circuit-level and signal processing techniques have been proposed to improve that energy efficiency. However more disruptive improvement can be achieved at system-level, capitalizing on energy-scalable design and circuit reconfiguration to match the user requirements and operation environment. We describe the design of such an energy-scalable reconfigurable transmitter as well as its control strategy. Based on measurement carried out on the physical realization of this transmitter, the benefit of system-level energy management is shown. Energy-efficiency scalability ranges over 30%, which translates in an average system-level energy improvement of up to 40% compared to a non-scalable system.

Categories and Subject Descriptors
B.7.0 [**Integrated circuit**]: *General*

General Terms
Design, Measurement, Performance, Theory.

Keywords
OFDM, Energy Management, Energy-aware design, Energy-scalability.

1. INTRODUCTION
Thanks to its robustness over harsh frequency selective channels combined with a relatively low complexity of its digital receiver, multi-carrier modulation such as Orthogonal Frequency Division Multiplexing (OFDM) has revealed to be a technique of choice for broadband transmission over wireless medium [1,2]. Therefore, OFDM is omnipresent in modern wireless interface standards – such as IEEE 802.11a/g/n, DAB, DVB-S/T/H, and IEEE 802.16e – where it has enabled breakthrough in data rate and capacity.

However, from the mixed-signal perspective, OFDM's key advantages come at the cost of very low energy efficiency due to stringent linearity requirements on the analog transmitter, consequent to the very high peak to average ratio of the OFDM signal [3]. Although this low power efficiency has been accepted so far, the current trend to have broadband wireless support in energy-limited portable devices such as PDA's and smartphones has triggered an urgent need of energy efficiency improvement.

Significant effort has already been spent to increase the energy efficiency of mixed-signal OFDM transmission chains mostly by reducing the OFDM signal peaks both in the digital and the analog domain. Yet, the power efficiency of state-of-the-art chipsets - defined as the ratio of the output power to the total power consumed by the transmitter circuitry - hardly reaches 20% in the 2.4GHz band [4] and 15% in the 5GHz band [5] for IEEE 802.11g standard compliant transmission.

Further improving the energy efficiency of OFDM transmitters needs to take the problem from a system-level perspective involving not only the digital and analog transmitter design but also considering end-to-end cross-layer interactions. In [6] and enclosed references, it is shown that applying a link-layer lazy scheduling policy [7] to the design of broadband wireless system has the potential to improve by 50 to 200% the energy-efficiency measured in energy per bit. Clearly, this is much better than what can be expected from waveform manipulation or pure analog circuit improvement.

However, the proposed approach builds on a postulated energy-scalable reconfigurable analog transmitter that depicts a controllable tradeoff between its performance - in terms of output power and linearity - and its DC power consumption. In this paper, we present an OFDM transmitter design which effectively presents these characteristics. Further, we reevaluate the gain of the energy-management approach presented in [6] based on measurements performed on the designed circuit.

The remainder of this paper is organized as follows. In section 2, we review the energy efficiency issue in OFDM transmitters and survey the state-of-the-art approaches to improve it. In section 3, the applied energy-scalable design methodology is described. The resulting design of the analog chip and the software controller are described in section 4 while the reevaluation of the system-level energy management approach of [6] is carried out in section 5. Conclusions are drawn in section 6.

2. ENERGY EFFICIENCY OF OFDM
2.1 Peak-to-average Power Ratio
The OFDM signal is modulated around a set of sub-carriers uniformly distributed in the targeted transmission band. This yields high robustness against frequency selectivity when combined with error correction codes and, by padding a cyclic prefix, mitigates inter-symbol interference, enabling very simple equalization [8].

The drawback of OFDM can however easily be visualized when considering the time-domain signal. The basic expression of an OFDM baseband signal is given by:

$$x[n/L] = \frac{1}{\sqrt{N}} \sum_{m=-\infty}^{+\infty} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}-1} X_k^m e^{j2\pi kn/NL} w_{CP}[(n - m(N+v)L)/L] \qquad (1)$$

where X^m_k is the complex representation of the QAM symbol modulating the sub-carrier k in the symbol m, N is the number of sub-carriers and L is the over-sampling factor (4 in practical design [1]). $w_{CP}[n/L]$ represents a rectangular window over the interval $[-vL, NL]$, v being the cyclic prefix length. Within any given symbol, the N sub-carriers phases $\arg(X_k^m)e^{j2\pi kn/NL}$ can potentially be the same, so that the sub-carriers add up constructively leading to a worst-case signal peak to average power ratio (*PAPR*) proportional to the number of sub-carriers.

$$PAPR\{x[n/L]\} \leq N \frac{\max\left|X_k^m\right|^2}{E\left\{\left|X_k^m\right|\right\}} \qquad (2)$$

For example, with 64 64QAM-modulated carriers, the worst case *PAPR* reaches 10.log(52) = 17.16 dB.

Due to this high *PAPR*, the analog transmitter should provide linear behavior across a large dynamic range. Such behavior is offered by class-A and class-AB amplifier architectures with maximum power efficiency of, respectively, 50 and 74%. These theoretical efficiencies, however, assume amplification of a sinusoid with a peak-to-peak swing over the entire amplification range. The effective efficiency degrades drastically (down to 10%) when considering amplifying signals with a large *PAPR*. Therefore, *PAPR* reduction and linearization techniques have been developed.

Non-linear amplification of a multi-carrier signal causes both harmonic and inter-modulation distortion. Harmonic distortion, which generates signal replica at the harmonic frequencies, is of low concern in single-band RF transmitters due to their band-selectivity. Inter-modulation distortion however generates inter-modulation products between the different sub-carriers, causing both in-band and out-of-band distortion. Because in OFDM the sub-carriers are equally spaced, the inter-modulation products hamper the signal to noise and distortion ratio (*SiNAD*) of each sub-carrier and hence increase the end-to-end bit error rate. The non-linear behavior of an amplifier is typically characterized by its output *1-dB* compression point (P_{1dB}). The P_{1dB} is defined as the power at which the actual gain is *1 dB* lower than it would be if the amplifier would be perfectly linear. The P_{1dB} is the common reference to define the back-off (*BO*) with respect to the average signal power. Both the P_{1dB} and the back-off can be in- and output referred, which yields the notations IP_{1dB}, OP_{1dB}, *IBO* and *OBO*.

Based on this framework, both *PAPR* reduction and linearization techniques can be evaluated in terms of performance. In the following, we survey the most effective techniques [9-15].

2.2 Energy efficiency enhancement

Linearization of analog circuits

Numerous linearization techniques for non-linear analog circuits have been proposed. Most of the conventional linearization techniques, such as negative feedback, do not apply for radio frequency (RF) applications. Remaining techniques applicable for OFDM can be classified in non-linear calibration and signal decomposition.

Non-linear calibration architectures and techniques have been proposed [14] to improve the overall system linearity by calibrating the analog circuit non-linearity and to - analog or digitally - pre-distort the input signal accordingly. This technique reduces the required back-off while improving the power efficiency with about 10% [11]. However, large signal peaks push the non-linear circuit into very deep saturation, losing its memory-less characteristics and hindering proper operation.

The other class of linearization techniques is based on signal decomposition. Numerous approaches have been described; generally, the signal is decomposed and individually treated efficiently. Examples are envelope elimination and recombination (EER) [13], linear amplification with non-linear components (LINC) [15] and Doherty [12]. In EER, the RF signal is decomposed in its envelope and phase component. The envelope signal can be amplified efficiently, even with a large *PAPR*, due to its low frequency. The phase can be treated non-linearly as its envelope is irrelevant. In LINC, the RF signal is decomposed in two or more constant-envelope signals that can individually be amplified in a non-linear way. In Doherty, the RF signal is sliced up according its instantaneous envelope and amplified accordingly.

These signal decomposition techniques drastically improve the efficiency versus back-off characteristic but they are subject to three major issues. First, the decomposition of the OFDM signal into well-suited components is not trivial and generally comes with a significant additional baseband processing cost. Secondly, the different analog paths have to match, which is far from trivial to realize at design time. Finally, the duplication of the up-conversion and/or amplification path leads to doubling the area cost, which is unacceptable in the highly competitive wireless market. This explains why these techniques are hardly deployed in practice.

Digital PAPR reduction

In the digital domain, numerous *PAPR* reduction techniques have been proposed to relax the constraints on the analog circuit design. Roughly, they can be classified in two categories: techniques with and without distortion. The first category reduces the *PAPR* by applying reversible transformations while the second trades-off *PAPR* and distortion. As distortionless techniques require modification in the digital transceiver hampering standard compliance, they are not considered in practice.

The most common digital *PAPR* reduction technique with distortion is successive clipping and filtering [16]; by successively clip and filter the signal in the digital domain, both the *PAPR* and the out-of-channel emission is reduced. However, convergence and optimality cannot be guaranteed. Moreover, this approach fails to meet the spectral mask for high-order modulation schemes s.a. 64QAM. A more attractive technique for *PAPR* reduction with distortion has recently been proposed [9,10]. The idea is to optimize the *PAPR* symbol-by-symbol, in the digital domain, under *EVM* (Error Vector Magnitude) constraint. It is shown in [9] that the aforementioned optimization is convex and can therefore be carried out with simple methods, leading to *OBO* requirements reduction by 4 to 6 dB for IEEE 802.11a. as depicted in Table 1.

Table 1. Requirements for the different IEEE802.11a signaling modes

Carrier modulation	Rate [Mbps]	EVM_{tx} [dB]	$SiNAD_{link}$ [dB]	Residual PAPR [15] Mean/Std. Dev. [dB/dB]	OBO [dB]
BPSK	6	-5	-0.3	0.7/.2	1.3
BPSK	9	-8	2.3	1.4/.4	2.6
QPSK	12	-10	2.8	1.9/.3	2.8
QPSK	18	-13	5.3	2.6/.3	3.5
16QAM	24	-16	8.3	3.1/.4	4.3
16QAM	36	-19	11.7	3.5/.4	4.7
64QAM	48	-22	15.9	3.8/.5	5.3
64QAM	54	-25	17.3	4.1/.5	5.6

3. METHODOLOGY FOR ENERGY-SCALABE TRANSMITTER DESIGN

The idea of energy-scalable system design [17] is, rather than designing a system based on static, low-power components, to assemble components that present a controllable tradeoff between their performance (e.g. precision, speed …) and their steady power consumption. Based on this flexibility, the system can adapt to the dynamic environment and use conditions, which avoid worst case dimensioning and globally yields average power consumption benefits. In [6,7,18], a methodology is proposed to apply the energy-scalable design paradigm to OFDM-based broadband wireless systems.

A set of parameters that influence the system-level energy efficiency and performance – namely, the modulation and coding rate, transmit power, transmitter linearity and receiver processing gain – have been identified. Using these parameters as *control knobs*, energy management policies are systematically derived at design-time and calibrated at run-time to adapt the system configuration to the actual user requirements (e.g. average packet rate and/or latency) and environment parameters (such as channel attenuation and frequency selectivity), yielding up to 10x energy efficiency improvement in realistic network conditions [18].

From the analog transmitter perspective, the relevant control knobs are the transmit power and performance (quantified as signal to distortion ratio, mainly depending on the back-off). Thanks to the *PAPR* reduction technique presented above [9,10], the back-off requirements decrease with the sub-carrier modulation order and, hence, the transmission rate. Table 1 shows these requirements for the different IEEE 802.11a signaling modes (carrier modulation and channel coding rate). The transmitter *EVM* constraints are given by the standard while the signal-to-noise and distortion ratio (*SiNAD*) requirement over the complete end-to-end link is derived from system simulations considering a packet error rate less than 10% with packet a size of 1000 bytes. Given an input referred equivalent receiver noise of -86dBm (thermal noise of -101dBm, receiver noise figure of 10dB and 5dB implementation margin), the required transmit power (P_{tx}) is derived for various path-loss (Figure 1). The sum of the transmit power (P_{tx}) and the output back-off (*OBO*) corresponds to the required output *1dB* compression point (OP_{1dB}) constraint.

For a fixed path-loss, both the required transmit power and the back-off constraint relax when the sub-carrier modulation - hence the transmission rate - decreases. This results in significant potential for energy-scalability, as it enables applying the link-layer lazy scheduling policy as described in [7]. However, this potential benefit is conditioned to the availability of transmitter circuits that allows trading off, in a controlled way, transmit power and back-off against power consumption. In the following, we present a flexible transmitter design that allows this tradeoff at design- and run-time.

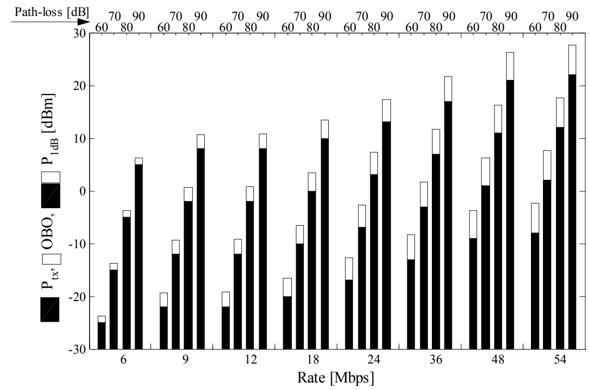

Figure 1. Rate versus required transmit power (P_{tx}), output back-off (*OBO*) and transmitter non-linearity (P_{1dB})

4. FLEXIBLE TRANSMITTER DESIGN

4.1 Circuit Design

A complete transceiver has been designed, including IEEE802.11a compatible digital modem [1] and zero-IF analog front-end. The analog front-end (excluding the power amplifier) is implemented in 0.35µm 3V SiGe BiCMOS technology. The system-level block diagram of the analog transmitter front-end is depicted in Figure 2 and consists of the following three stages: an I/Q direct-upconversion mixer, a driver amplifier (DA) and an external power amplifier (PA).

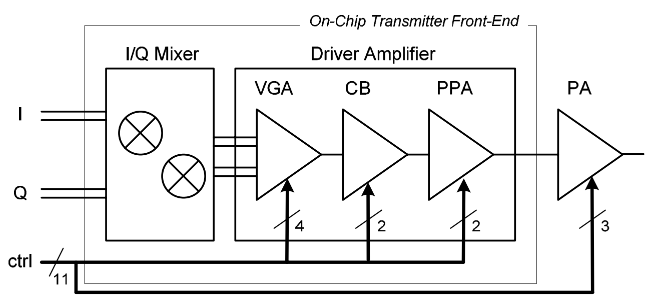

Figure 2. System level block diagram of the analog transmitter front-end

The **I/Q direct-upconversion mixer** is a differential Gilbert-cell mixer that combines the in-phase (I) and the quadrature (Q) baseband signals into an RF signal.

The **driver amplifier** consists of a cascade of a variable gain amplifier (VGA), a current buffer (CB) and a power amplification stage (PPA). Simplified circuit diagrams are shown in Figure 3. To limit the power consumption, a mainly single-ended topology was chosen.

The VGA consists of two amplification stages converting the differential signal to a single-ended signal: a differential pair amplifier with emitter degeneration and a single-ended emitter follower. Two current sources were used on each side of the degeneration resistance to avoid the voltage drop across this resistance which would be the case if a single current source would the connected to the center of the resistance. Avoiding this voltage drop increases the input dynamic range of the amplifier. The output of the linearized differential amplifier is then buffered using a single-ended emitter follower. This buffering is required to bridge the output impedance of the differential amplifier to the input impedance of the following amplification stage.

The goal of the current buffer, CB, is to deliver the necessary current to the following stage. The topology used in this buffer is single-ended emitter degeneration with resistive load. A resistive load is favorable above an active one when using this topology in RF applications. The reasons for this are: first, it simplifies biasing of the buffer transistor. Second, corner simulations indicate large performance sensitivity when using an active load (its resistance - thus the gain of the circuit - and its parasitics strongly depend on process variation). Finally, an active load requires a relatively high voltage drop to operate properly. This voltage drop limits the remaining voltage swing and thus limits the linearity of the circuit. Linearity should be preserved in the buffer to avoid saturation before following amplification stages saturate. Therefore, a resistive load will be used in the current buffer.

The main goal of the PPA is to deliver the required current to drive the external PA. This is done by using a typical class-A amplifier with an on-chip inductive load. A small emitter resistor has been introduced to combat thermal runaway. The voltage drop over the resistor is limited to reduce the loss in power efficiency. The stability of the amplifier is guaranteed by adding a RC stabilization network between the base and the collector of the transistor.

The **external power amplifier** is an off-chip commercial device: the Microsemi LX5503 power amplifier has been used [19]. This device, manufactured in an InGaP/GaAs heterojunction bipolar transistor technology, contains a dual-stage amplifier with active bias and is dedicated to high gain linear amplification in the 4-6GHz band.

Both the driver amplifier and power amplifier are made flexible in terms of performance - output power and linearity - and DC power consumption. The digital lines to control this flexibility have been indicated in Figure 2. Simplified circuit diagrams of the flexible stages are shown in Figure 3. Four techniques to change the circuit characteristics have been applied:

- Tunable degeneration resistance; impacts both the amplification gain and linearity
- Tunable load resistance; mainly impacts the amplification gain
- Tunable bias current or voltage; impacts the DC power consumption and the performance
- Tunable supply voltage; impacts the DC power consumption and the performance

The physical realization of the transmitter has been mounted together with the power amplifier on a high-frequency PCB, which is embedded in a real time prototyping system [20]. The DC power consumption (*Pdc*) and the output spectrum have been measured for each transmitter configuration with a dual-tone input signal. The transmitter performances metrics, namely the output power (P_{tx}) and the signal to noise and distortion ratio ($SiNAD_{tx}$), have been extracted from the measured spectra. As transmitter imperfections such as carrier leakage and quadarture imbalance

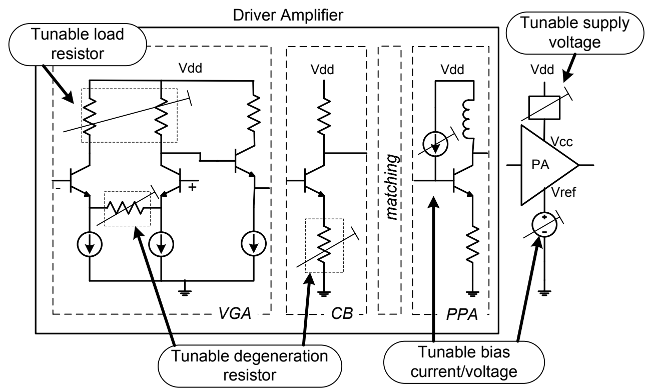

Figure 3. Simplified circuit diagrams of the flexible front-end blocks

are compensated for [21], the distortion is mainly caused by nonlinear amplification in the transmitter system. Figure 4 illustrates the measured performances (P_{tx}, $SiNAD_{tx}$) and DC power consumption (P_{dc}) for each of the 2048 (= 2^{11}) transmitter configurations.

Obviously, this large amount of transmitter configurations cannot be all calibrated at run-time. Moreover, lots are sub-optimal. To efficiently use the transmitter flexibility, a thorough design-time pruning and run-time calibration and control are needed.

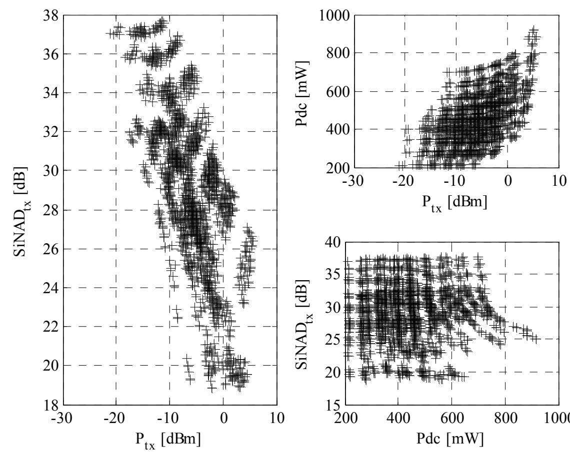

Figure 4. Measured analog transmitter front-end performance, in terms of output power (P_{tx}) and signal purity (*$SiNAD_{tx}$*), and DC power consumption (*Pdc*) for each of the 2048 transmitter configurations.

4.2 Design-time pruning and run-time control

As depicted in Figure 4, the proposed circuit flexibility provides transmit power and *SiNAD* performance versus DC power tradeoff. However, numerous of the possible settings still correspond to sub-optimal operation. Next to the actual transmitter circuitry, a controller has to translate the high-level transmit power and linearity requirement in optimal circuit settings. This translation is done in two systematic phases:

First, at design-time, the configurations leading to sub-optimal operation in the P_{out} – $SiNAD_{tx}$ - P_{DC} triplet multi-objective space are pruned out. To do so, our methodology involves identification of the three dimensional convex hull of the cloud of possible working points (configurations); several effective techniques are available in literature for this hull computation. The triplet points on this hull that satisfy the Pareto optimality criterion [22] are kept. The Pareto optimality criterion guarantees that for a remaining working point, it is impossible to improve the performance in one or the other direction (transmit power or linearity) without increasing the DC power. This operation reduces the potentially useful transmitter configurations in this design from 2048 down to 83.

Further pruning is possible at calibration time provided that the average path-loss (*PL*) is known. Based on the link budget relation in (3), the link *SiNAD* can be computed as a function of the transmitter *SiNAD*, the transmit power (P_{Tx}) and the input referred equivalent receiver noise (N_{rx}), which consist of the receiver's thermal noise ($N_{thermal}$=*-86dBm* for IEEE802.11a bandwidth at room temperature), its noise figure (NF_{rx}) and its distortion.

$$\frac{1}{SiNAD_{link}} = \frac{1}{SiNAD_{tx}} + \frac{N_{rx} \times PL}{P_{tx}} \tag{3}$$

$$N_{rx} = N_{thermal} \cdot NF_{rx} \cdot IM \tag{4}$$

For ease of illustrating further pruning, N_{rx} is considered independent of the received signal power. In practical systems, however, the variable gain stages of the receiver will be configured according to the signal power at the antenna. This affects the receiver noise figure and distortion. Although the methodology can handle variable receiver noise, it will be illustrated with an IEEE802.11a-realistic noise figure and implementation margin (IM) of 10dB and 5dB respectively.

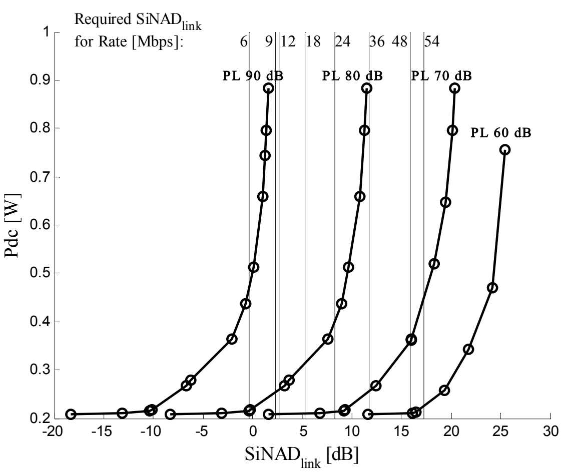

Figure 5. Power consumption of the transmitter front-end (*Pdc*) versus *SiNAD$_{link}$* trade -off for various path-loss

Based on the link budget (3-4), one can carry out the optimization of the tradeoff between the effective link performance metric, namely the $SiNAD_{link}$ and the transmitter power consumption. The resulting convex relations are reproduced in Figure 5 for an average path-loss ranging from 60 to 90 dB. It remains around 10 working points per curves. Those are well distributed across the tradeoff range, making the energy-scalable transmitter usable for system-level energy management. With a path-loss of 80 dB for instance, when configured to transmit at 36Mbps (16QAM, code rate 3/4), the transmitter energy consumption is 25nJ/bit while it scales down to 16,6nJ/bit (33% improvement) when configured for 24Mbps transmission (16QAM, code rate 1/2). Similarly, with a path-loss of 70 dB, the energy consumption scales from 9,25nJ/bit at 54Mbps down to 6.94nJ/bit at 36Mbps (25% improvement).

Given circuit-level energy-flexibility comes at limited increase of area cost and circuit complexity. The main challenge of cost optimization relies in the run-time calibration strategy. This involves calibration of the transmitter and receiver circuit performance and acquisition of the environmental conditions, e.g. path loss, in a standard compliant efficient and -probably- combined way. This cost optimization opportunity is currently investigated. Fortunately, the monotonic nature of the Pareto curves derived at design-time allows addressing this cost optimization systematically and effectively.

5. IMPACT ON SYSTEM-LEVEL ENERGY MANAGEMENT

Based on the transmitter architecture and its control subsystem presented above, the system-level energy management technique postulated in [6] can be applied in practical systems. In this section, we reevaluate the system-level net average rate versus energy efficiency tradeoff based on the transmitter measurement figures presented above.

The basic principle of the considered energy management scheme is to jointly adapt to the transmission channel, by link adaptation [23] and to the traffic requirements, by lazy scheduling [24]. As explained in detail in [7], the link adaptation and packet scheduling policies are derived capitalizing on the convex relation between *SiNAD* and energy efficiency provided by the scalable transmitter. This yields a tradeoff between the average net data rate and the energy efficiency. The tradeoff range obtained with the designed transmitter is illustrated in Figure 6 for different path-losses. An IEEE 802.11a compliant transmission scheme and medium access protocol is considered. Packet arrival is assumed periodic with constant rate (Constant Bit Rate - CBR - traffic)

Compared with traditional WLAN radio link control (RLC) schemes, where the data is transmitted as fast as possible (at the maximum data-rate achievable on the actual channel) and the transmitter is shut down when no data has to be sent, the proposed scheme improve the energy efficiency by up to 40%

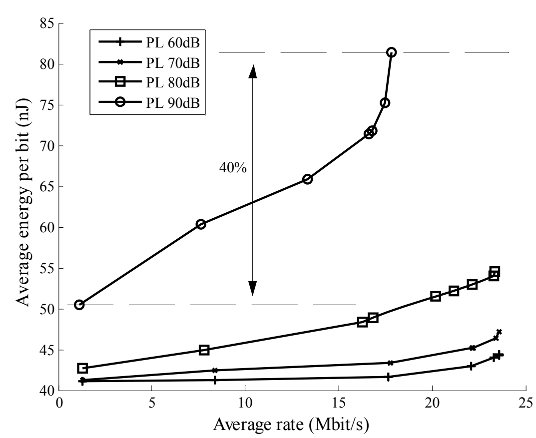

Figure 6. System-level energy efficiency versus average data-rate tradeoff obtained based on the proposed energy-scalable transmitter

6. CONCLUSION

Orthogonal Frequency Division Multiplexing (OFDM) revealed to be a modulation of choice for multiple broadband wireless communication standards including IEEE 802.11a/g, IEEE 802.16, DAB and DVB-T/H. However, this good performance comes at the cost of a very low energy efficiency of the analog transmitter. Numerous circuit-level and digital signal processing techniques have been proposed to improve that energy efficiency but their gain stay limited. In previous work, it has been shown that more disruptive energy efficiency improvement can be achieved at system-level capitalizing on energy-scalable reconfigurable circuit and system design combined with run-time control adapting to user requirements and operation environments. Yet, those results build on the availability of a transmitter that depicts a controllable tradeoff between its output power, its linearity and its power consumption. The design of such a transmitter for 5GHz OFDM is still a challenge. In this paper, we have described an architecture for such an energy-scalable transmitter as well as its control strategy. Based on measurement carried out on the physical realization of the transmitter, the benefit of the aforementioned system-level energy management technique has been reevaluated. It is shown that the proposed transmitter presents an energy-scalability range up to 30%, which translate in average system-level energy efficiency improvement of up to 40%. The presented work is currently expanded to the design of multi-mode software-defined radio transmitter.

7. ACKNOWLEDGMENTS

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