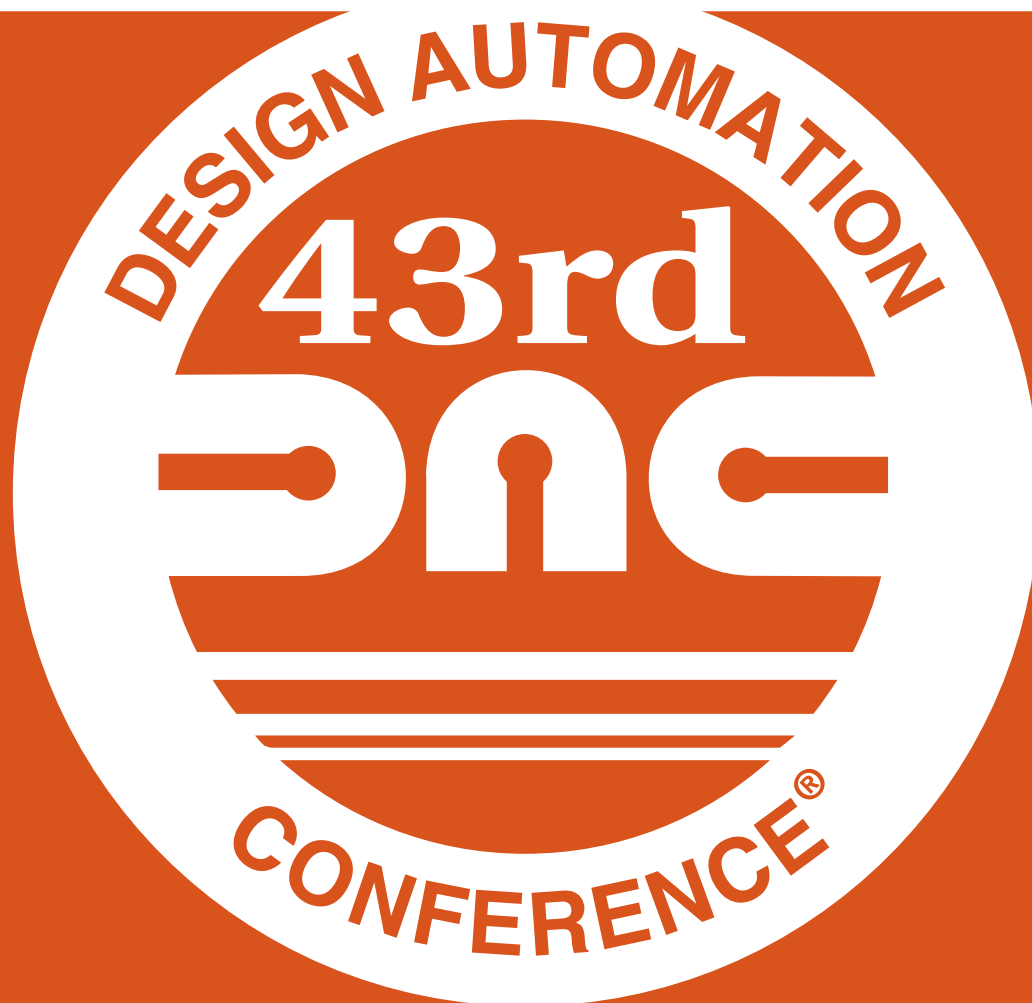


PROCEEDINGS 2006

DESIGN AUTOMATION CONFERENCE



The Moscone Center
San Francisco, CA, July 24-28, 2006

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GENERAL CHAIR'S WELCOME

Welcome to San Francisco and the 43rd Design Automation Conference! San Francisco is an excellent venue for DAC, with its proximity to many high-tech companies, its beautiful location, and a wide variety of activities and sights. DAC's return to San Francisco after eight years of absence promises a lively and especially well-attended event. Thousands of executives, managers, designers, academics, journalists, and others are converging here during DAC, the largest and most prestigious event focused on the design of electronic circuits and systems.

The technical program, which received a record 865 regular paper submissions, includes hot topics such as low power, DFM, and ESL among many others. This year, it sees an increase in design papers and includes two new topics: beyond-the-die, and emerging technologies. Overall, the program contains more than 200 technical presentations in 11 tracks, eight technical program panels, seven special sessions, and seven full-day tutorials – all led by widely respected industry experts. Full-day tutorials are being held Monday and Friday, and cover a wide range of topics including DFM, verification, ESL, embedded systems, chip-package co-design, and test.

DAC is highlighting a special MEGa theme – Multimedia, Entertainment, and Games – found throughout the program in all three keynotes, several pavilion sessions, and in a full day of technical sessions on Wednesday. Topics will range from issues faced in the design of the iPod, to technology requirements for 3D graphics in feature films, to power management for next-generation media applications. This promises to be an exciting part of the program as the topic is timely, exposes cutting-edge problems, and touches everyone's lives.

Three keynote addresses will be held this year. Monday's keynote is Joe Costello, appearing nearly 10 years after leaving his post as Cadence's CEO. His recent endeavor has been serving as Chairman of Orb Networks, Inc., a company working to bring media to mobile devices, and his talk will focus on today's macro consumer trends. Tuesday's keynote is Hans Stork, Senior Vice President and CTO of Texas Instruments Inc., who brings a wealth of experience and knowledge in process technologies. He will address issues in the sub-50nm processes that enable SoCs in mobile communication devices of the future. On Thursday, DAC welcomes Alessandro Cremonesi, VP of Strategy and System Technology and General Manager of Advanced System Technology at STMicroelectronics, who has been leading ST's efforts in SoC design. He will deliver a keynote on the challenges of convergence – handling the increased complexity at the system, embedded software, and silicon implementation level.

DAC has again organized Management Day to be held Tuesday, offering mid- and senior-level design managers a forum for sharing information on technology trends and decision-making processes.

The exhibit floor is crowded and will be lively with more than 240 exhibitors. On the floor, be sure to visit the DAC pavilion which returns with a full schedule of 18 panels, the MEGa theme booth with exciting demos, and the networking opportunities at the Monday exhibit floor happy hour. Hands-on tutorials given by exhibitors are scheduled throughout the week, all covering low-power design.

DAC promises to be a great learning experience. Advancements, research and insights that the global design community brings to this year's event has something to interest everyone.

It is the contributions of many people that make DAC the success that it has been for over four decades as the premier design automation event. The technical program participants and the many volunteer committees work to provide the core of the program content and direction for future years. Conference Managers MP Associates, Inc. continue to be focused on DAC's success. We are grateful for the support of our sponsors, ACM/SIGDA, IEEE/CASS/CANDE/CEDA, and the EDA Consortium.

Enjoy an educational and exciting week at DAC in San Francisco!



Best regards,
Ellen Sentovich
General Chair, 43rd DAC

PROCEEDINGS OF THE 43RD DESIGN AUTOMATION CONFERENCE®

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EXECUTIVE COMMITTEE



GENERAL CHAIR

Ellen M. Sentovich
Cadence Berkeley Labs
1995 University Ave. Ste. 460
Berkeley, CA 94704
510-647-2807
ellens@cadence.com



VICE/FINANCE CHAIR

Steven P. Levitan
University of Pittsburgh, ECE Dept.,
348 Benedum Eng. Hall
Pittsburgh, PA 15261
412-648-9663
steve@ee.pitt.edu



TECHNICAL PROGRAM CO-CHAIR (METHODS)

Grant E. Martin
Tensilica, Inc.
3255-6 Scott Blvd.
Santa Clara, CA 95054
408-327-7323
gmartin@tensilica.com



TECHNICAL PROGRAM CO-CHAIR (TOOLS)

Sachin Sapatnekar
University of Minnesota
200 Union St., 4-174 EE/CSI
Minneapolis, MN 55455
612-625-0025
sachin@ece.umn.edu



EDA INDUSTRY CHAIR

Limor Fix
Intel Research Pittsburgh
4720 Forbes Ave., Ste. 410
Mailstop CM2
Pittsburgh, PA 15213
412-297-4021
limor.fix@intel.com



PAST CHAIR

William H. Joyner, Jr.
IBM Corp./SRC
PO Box 12053
Research Triangle Park,
NC 27709
919-941-9472
william.joyner@src.org



TUTORIAL CHAIR

Leon Stok
IBM Corp.
2070 Route 52
Hopewell Junction, NY 12533
845-892-5262
leonstok@us.ibm.com



PANEL CHAIR

Dennis Brophy
Mentor Graphics Corp.
8005 SW Boeckman Rd., Bldg. E4
Wilsonville, OR 97070
503-685-0893
dennisb@model.com



DESIGN COMMUNITY CHAIR

Ingrid Verbauwhede
Katholieke University
Kasteelpark Arenberg 10
Leuven, Belgium
+32-16-32-86-25
ivebauw@esat.kuleuven.be



NEW INITIATIVES CHAIR

Andrew B. Kahng
Univ. of California at San Diego
CSE & ECE Depts. 0114
9500 Gilman Dr.
La Jolla, CA 92093
858-822-4884
abk@cs.ucsd.edu

EXECUTIVE COMMITTEE (Continued)



PUBLICITY CHAIR
Nanette V. Collins
Public Relations Consultant
37 Symphony Rd., Unit A
Boston, MA 02115
617-437-1822
nanette@nvc.com



EUROPE/MIDDLE EAST REPRESENTATIVE
Ahmed A. Jerraya
TIMA Lab
46, Avenue Felix Viallet
Grenoble Cedex, France F-38031
+33 476-574759
ahmed.jerraya@imag.fr



ASIA/SOUTH PACIFIC REPRESENTATIVE
Yusuke Matsunaga
Kyushu University
6-1 Kasuga Koen
Kasuga, Fukuoka
816-8580, Japan
+81 92-583-7621
matsunaga@c.csce.kyushu-u.ac.jp



ACM/SIGDA REPRESENTATIVE
Diana Marculescu
Carnegie Mellon University
EEC Department - HH #2124
Pittsburgh, PA 15213
412-268-1167
dianam@ece.cmu.edu



IEEE/CASS/CANDE REPRESENTATIVE
Alan Mantooth
University of Arkansas
Dept. of EE
3217 Bell Engineering Center
Fayetteville, AR 72701
479-575-4838
mantooth@uark.edu



EDA CONSORTIUM REPRESENTATIVE
Anne Cirkel
Mentor Graphics Corp.
8005 SW Boeckman Rd.
Wilsonville, OR 97070
503-685-7934
anne_cirkel@mentorg.com



CONFERENCE MANAGER
Kevin Lepine
MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
303-530-4562
kevin@mpassociates.com



EXHIBITS MANAGER
Lee Wood
MP Associates, Inc.
5405 Spine Rd., Ste. 102
Boulder, CO 80301
303-530-4562
lee@mpassociates.com

TECHNICAL PROGRAM COMMITTEE

Grant E. Martin
Technical Program Co-Chair
Tensilica, Inc.
gmartin@tensilica.com

Sachin Sapatnekar
Technical Program Co-Chair
University of Minnesota
sachin@ece.umn.edu

Brian Bailey
Consultant
Oregon City, OR

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Mentor Graphics Corp.
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Denton, TX

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Boulder, CO

MONDAY KEYNOTE ADDRESS



Joe Costello
Chairman of the Board,
Orb Networks, Inc.

iPod or Iridium – Which One Are You Going To Be?

Abstract: An incredible amount of time, resources and investment is being made by EDA, chip, and electronics companies to win in the exploding multi-media, gaming, and entertainment applications markets. With the 2006 DAC conference doing a much-needed “deep dive” into how the semiconductor industry meets technical challenges, Joe Costello, Chairman of Orb Networks, Inc., will turn the spotlight away from technology and onto today’s macro consumer trends.

During this session, Joe challenges participants with this fundamental question: are you going in the right direction? As you bend your minds with the complexity of implementing modern day systems and chips, are you racing toward the right finish line? What are consumers really looking for? What will convergence really lead to and are you positioned to take advantage of all it will bring our industry and our world? Join Joe as he reveals lessons learned and offers a simple view of the future of electronics.

Biography: Joe Costello is chairman, co-founder, and an investor in Orb Networks, Inc. He is highly regarded for his business acumen and bold moves in the high-tech industry. In 1997, Chief Executive Magazine named Costello the top performing CEO of all publicly traded companies in North America. He also made Upside Magazine’s 1997 “Elite 100” list of the top executives leading the digital revolution. He serves as CEO and chairman of think3, a developer of computer-aided design software used throughout the product development process. He is also chairman of other privately-held companies that include Radio, Abazab and SpeakESL. In addition, Costello is on the board of Mercury Interactive, a publicly-held company. Prior to think3, Costello played a pivotal role as president and CEO at Cadence Design Systems, Inc. for more than a decade. Under his leadership, Cadence became the world’s leading supplier of electronic EDA software and services, and one of the ten highest-grossing software vendors in the world. Costello holds a bachelor of science degree in mathematics and physics from Harvey Mudd College, a master of science degree in physics from Yale University, and a master of science degree in physics from the University of California, Berkeley.

GENERAL SESSION KEYNOTE ADDRESS



Hans Stork

Senior Vice President and Chief Technology Officer,
Director of Silicon Technology Department
Texas Instruments Inc.

Structuring Process and Design for Future Mobile Communication Devices

Abstract: The density and speed of sub-50nm CMOS technology enables the design of multi-functional SoCs for highly integrated, mobile, communication devices. At the same time, process variations, power issues and complexity of scope are challenging even the most advanced simulation capabilities. The growing design complexity is addressed by rapidly improving modeling of systematic manufacturing variations and design sensitivities. Physical design is becoming more structured to allow for process optimized design rules and efficient automation. While challenges remain in the scaling and optimization of analog and I/O functions, highly integrated, mobile communication devices are a major driving force for continued economies of scaling.

Biography: Dr. Stork is Senior Vice President, and Chief Technology Officer, of Texas Instruments. As Director of the Silicon Technology Development organization, he is responsible for ensuring that process technology provides a competitive advantage for TI's products.

Prior to joining Texas Instruments in 2001, Dr. Stork was Director of the ULSI Research Lab and later the Internet Systems and Storage Lab at HP Laboratories, Hewlett-Packard. Dr. Stork started his professional career at IBM's T.J. Watson Research Center, working on advanced bipolar technology and circuits, and his group demonstrated the early successes SiGe HBTs.

Dr. Stork serves on the Board of Directors for International Sematech and the Semiconductor Research Corporation (SRC). He also serves on the Governing Councils of the Focus Center Research Programs and Nanotechnology Research Initiative. He is a member of the SIA Technology Strategy Committee.

THURSDAY KEYNOTE ADDRESS



Alessandro Cremonesi

Strategy and System Technology Group Vice President
and Advanced System Technology General Manager,
STMicroelectronics

The Challenges of Convergence

Abstract: In this talk, the trends of the major application fields in the era of convergence are analyzed. The emphasis is on the challenges the semiconductor industry will have to face to address these new trends and opportunities.

Applications are becoming increasingly complex and the need to guarantee the coexistence of a wider range of applications on a single chip makes system-level integration a real challenge. Most of the applications will run on platforms designed for portable products, pushing the industry to emphasize power budgets for new designs, both at silicon and at system level. From the platform architecture perspective, multiprocessing is already a reality and the industry will have to find new paradigms to handle the increased complexity at the system, embedded software, and at the silicon implementation level.

The talk concludes with future perspectives, from the viewpoint of ST's advanced research organization.

Biography: Alessandro Cremonesi received a Doctorate in Electronics Engineering from the University of Pavia, Italy, in 1984. After a period of research activity in the opto-electronics field at the University of Pavia, he joined STMicroelectronics working in different fields from telecommunications to audio/video digital signal processing and multimedia applications. At present, Alessandro Cremonesi is Vice President of Strategy and System Technology group and General Manager of Advanced System Technology (AST) group at STMicroelectronics with the responsibility of the Corporate System R&D and the Corporate Strategic Marketing activities across 14 different STMicroelectronics Labs worldwide.

Marie R. Pistilli Women in EDA Achievement Award

Ellen J. Yoffa – Director of Next Generation Web, IBM T.J. Watson Research Center, Yorktown Heights, NY

For her significant contributions in helping women advance in the field of EDA technology.

The P. O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship, and SIGDA continues to administer the program for DAC. DAC normally funds two or more \$4000 scholarships, renewable up to 5 years, to graduating high school seniors.

The 2006 winners are:

Katlyn DeLuca – attending University of Massachusetts, Lowell, MA

Eletha Flores – attending Massachusetts Institute of Technology, Cambridge, MA

For more information about the P. O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several \$24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in “design and test automation of electronic and computer systems.” Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. **Jennifer L. Dworak**, Division of Engineering – Electrical Sciences and Computer Engineering, Brown University, Providence, RI

Student: **Elif Alpaslan**

*A Statistical Coverage Metric and Stimulus Generation Approach for Design Verification
Based upon Structural Analysis of the Design and Stimulus*

Prof. **Daniel Kroening**, Computer Systems Institute, Swiss Institute of Technology, Zurich, Switzerland

Student: **Vijay D’silva**

Automatic Detection of Multi-Cycle Paths in Large Circuits

Information on next year’s DAC scholarship award program will be available on the DAC web site: <http://www.dac.com>.

DAC/ISSCC 2006 Student Design Contest Winners

Operational Chip Design Category:

- 1st Place** *A 10.6mW/0.8pJ Power-Scalable 1 GS/s 4b ADC in 0.18um CMOS with 5.8GHz ERBW*
- (Best Overall)** Pierluigi Nuzzo, Fernando De Bernardinis, Pierangelo Terreni – University of Pisa
Bert Gyselinckx, Liesbet Van der Perre, Geert Van der Plas – IMEC
- 2nd Place (tie)** *Increasing the Time Dynamic Range of Pulse Measurement Techniques in Digital CMOS*
Mona Safi-Harb, Gordon W. Roberts – McGill University
- 2nd Place (tie)** *A DSP Enabled Microsystem for Cochlear Implants with Hybrid LC Clocking*
Eric D. Marsman, Robert M. Senger – University of Michigan
Richard B. Brown – University of Utah
- 3rd Place** *A 160K Gates/4.5KB SRAM H.264 Video Decoder for HDTV Applications*
Chien-Chang Lin, Jia-Wei Chen, Hsiu-Cheng Chang, Chao-Ching Wang, Yi-Huan Ou-Yang, Ming-Chih Tsai, Yao-Chang Yang, Jiun-In Guo, Jinn-Shyan Wang – National Chung Cheng University

Operational System Design Category:

- 1st Place** *Demonstration of Uncoordinated Multiple Access in Optical Communications*
Herwin Chan, Andres I. Vila Cadaso, Juthika Basak, Miguel Griot, Wen-Yen Weng, Richard Wesel, B. Jalali, Eli Yablonovitch, Ingrid Verbauwhede – University of California, Los Angeles
- 2nd Place** *Illumimote: A High Performance Light Sensor Module for Wireless Sensor Networks*
Heemin Park, Jonathan Friedman, Mani B. Srivastava, Pablo Gutierrez, Vidyut Samanta, Jeff Burke – University of California, Los Angeles
- 3rd Place** *An Ultra Low Power Wireless Micro-Sensor Node*
Denis Daly, Daniel Finchelstein, Nathan Ickes, Naveen Verma, Anantha Chandrakasan – Massachusetts Institute of Technology
- Honorable Mention** *Phase Delay Based Collision Avoidance RADAR for Smart Automobiles*
Babu L. Saincha – Indian Institute of Information Technology

Conceptual Category:

- 1st Place** *ASIC Implementation of LDPC Decoder Accelerating Message-Passing Schedule*
Kazunori Shimizu, Tatsuyuki Ishikawa, Nozomu Togawa, Takeshi Ikenaga, Satoshi Goto – Waseda University

The ACM Transactions on Design Automation of Electronic Systems (TODAES) 2006 Best Paper Award

Zero Cost Indexing for Improved Processor Cache Performance
Volume 11, Issue 1, January 2006, Pages 3–25

Tony Givargis – University of California, Irvine, CA

The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) Distinguished Service Award

Robert A. Walker – Kent State University, Kent, OH

For dedicated service as SIGDA Chair (2001–2005), and over a decade of service to SIGDA, DAC, and the EDA profession

2005 Phil Kaufman Award for Distinguished Contributions to EDA

Phil Moorby – Chief Scientist, Synopsys, Inc.

Phil Moorby is the recipient of the prestigious EDA Consortium 2005 Phil Kaufman Award for industry contributions as the inventor of the Verilog hardware design language (HDL) which has become, and today remains, one of the world's most popular electronic design languages.

IEEE Circuits and Systems Society 2006 Education Award

Wayne Wolf – Princeton University, Princeton, NJ

For outstanding education and leadership in VLSI systems and embedded computing

IEEE Circuits and Systems Society 2006 Industrial Pioneer Award

John A Darringer – IBM T. J. Watson Research Center, Yorktown Heights, NY

For the development of practical techniques and algorithms for automated logic synthesis, for their realization as usable tools, and for their successful application to high performance computing products

IEEE Circuits and Systems Society 2006 Donald O. Pederson Award

Janusz Rajski – Mentor Graphics Corp., Wilsonville, OR

Jerzy Tyszer – Poznan University of Technology, Poznan, Poland

Mark Kassab – Mentor Graphics Corp., Wilsonville, OR

Nilanjan Mukherjee – Mentor Graphics Corp., Wilsonville, OR

For the paper entitled, *Embedded Deterministic Test*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 5, pp. 776–792, May 2004

IEEE Circuits and Systems Society 2006 CSVT Transactions Best Paper Award

Deepak Srinivas Turaga – Philips Research USA, Briarcliff Manor, NY

Mihaela van der Schaar-Mitrea – Philips Research USA, Briarcliff Manor, NY

Beatrice Pesquet-Popescu – Telecom Paris, Paris Cedex 13, France

For the paper entitled, *Complexity Scalable Motion Compensated Wavelet Video Encoding*, IEEE Transactions on Circuits and Systems for Video Technology, vol. 15, no. 8, pp. 982–993, August 2005

IEEE Circuits and Systems Society 2006 VLSI Transactions Best Paper Award

Amit Agarwal – Intel Corp., Hillsboro, OR

Bipul C. Paul – Purdue University, West Lafayette, IN

Hamid Mahmoodi – San Francisco State University, San Francisco, CA

Animesh Datta – Purdue University, West Lafayette, IN

Kaushik Roy – Purdue University, West Lafayette, IN

For the paper entitled, *A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 13, no. 1, pp. 27–38, January 2005

2006 IEEE Fellows

Charles Alpert – IBM Corp., Austin, TX

For contributions to physical design automation of very large scale integrated (VLSI) circuits

Wolfgang Kunz – University of Kaiserslautern, Kaiserslautern, Germany

For contributions to hardware verification, very large scale integrated (VLSI) circuit testing and logic synthesis

Resve Saleh – University of British Columbia, Vancouver, BC, Canada

For contributions to mixed-signal integrated circuit simulation and design verification

Chuan-Jin Richard Shi – University of Washington, Seattle, WA

For contributions to computer-aided design of mixed-signal integrated circuits

Martin Wong – University of Illinois at Urbana-Champaign, Urbana, IL

For contributions to algorithmic aspects of computer-aided design (CAD) of very large scale integrated (VLSI) circuits and systems

REVIEWERS

A record of 865 manuscripts were submitted to the 43rd DAC. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts. Our thanks to all of those who participated and contributed to the success of the Conference.

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Markus Seuring	Neal Stollon	Ram Vemuri	Mehmet Yildiz
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Nikhil Sharma	Mohd Sulaiman	Natesan Venkateswaran	Karen Yorav
Mary Sheeran	Savithri Sundaeswaran	Wim Verhaegen	F.Y. Young
Namrata Shekhar	Peter Sutton	Manish Verma	David Yu
Rupesh Shelar	Cliff C.N. Sze	Bart Vermeulen	Peng Yu
Shengyu Shen	Frank Szorc	Frederik Vermeulen	Wenjian Yu
Narendra Shenoy	Bassam Tabbara	Oreste Villa	Lin Yuan
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CALL FOR PAPERS



44th DESIGN AUTOMATION CONFERENCE® FOR INFORMATION CALL: 1-303-530-4333 San Diego Convention Center, San Diego, CA · June 4-8, 2007

DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. Panel and tutorial suggestions, and special session submissions are due **NO later than 5:00 pm MST, November 1, 2006**; Regular Papers are due **NO later than 5:00 pm MST, November 20, 2006**.

TOPICS OF INTEREST

DAC 2007 is seeking papers that deal with design tools, design methods, design techniques, and embedded design in a number of categories described below.

Design Tools papers describe contributions to the research and development of design tools and their supporting algorithms.

Design Methods and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

Design Papers describe the use of design tools and methods from the perspective of a specific design project. They include a brief description of the design and discussion of: methodology, flow, innovative use of tools, the limits of current tools, and what new tool capabilities are required for future designs.

Embedded Systems are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

The theme topic for DAC 2007 is automotive electronics, and papers that specifically refer to the theme will be highlighted at the conference.

Submitters are required to specify a category from the 18 listed below.

Categories:

1. System-Level Design and Co-Design

- 1.1 System specification, modeling, simulation, and performance analysis
- 1.2 Scheduling, HW-SW partitioning
- 1.3 IP and platform-based design, IP protection
- 1.4 System-on-Chip (SoC) and Multi-processor SoC (MPSoC)
- 1.5 Application-specific processor design tools

2. System-Level Communication and Networks on Chip

- 2.1 Modeling and performance analysis
- 2.2 Communications-based design
- 2.3 Architectural synthesis, mapping, routing, scheduling
- 2.4 Optimization for energy, fault-tolerance, reliability
- 2.5 Interfacing and software issues
- 2.6 NoC Design methodologies and CAD flows, case studies and prototyping

3. Embedded HW Design and Applications

- 3.1 Case studies of embedded system design
- 3.2 Flows and methods for specific applications and design domains

4. Embedded SW Tools and Design

- 4.1 Retargetable compilation
- 4.2 Memory/cache optimization
- 4.3 Real-time single- and multi-processor scheduling, linking, loading
- 4.4 Real-time operating system

5. Power Analysis and Low-Power Design

- 5.1 System level power design and thermal management
- 5.2 Embedded low-power approaches: partitioning, scheduling, and resource management
- 5.3 High-level power estimation and optimization
- 5.4 Gate-level power analysis and optimization
- 5.5 Device, circuit techniques for low-power design

6. Verification

- 6.1 Functional, transaction-level, RTL, and gate-level modeling and verification of hardware design
- 6.2 Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- 6.3 Emulation and hardware simulators or accelerator engines
- 6.4 Modeling languages and related formalisms, verification plan development and implementation
- 6.5 Assertion-based verification, coverage-analysis, constrained-random testbench generation

7. High-Level Synthesis

- 7.1 High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- 7.2 HW-SW interface synthesis, communication and network synthesis
- 7.3 Synthesis of digital circuits above the RTL level
- 7.4 Resource scheduling, allocation, and synthesis

8. Beyond Die-Integration and Package/Hybrid/Board Design

- 8.1 Chip-package-board co-design
- 8.2 System-in-Package, 3D design, stacked devices
- 8.3 Beyond-the-die communication, high-speed I/O, optical communication
- 8.4 Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

9. Logic Synthesis and Circuit Optimization

- 9.1 Combinational, sequential, and asynchronous logic synthesis
- 9.2 Library mapping, cell-based design and optimization
- 9.3 Transistor and gate sizing and resynthesis
- 9.4 Interactions between logic design and layout or physical synthesis

10. Circuit Simulation and Interconnect Analysis

- 10.1 Electrical-level circuit simulation
- 10.2 Model-order reduction methods for linear systems
- 10.3 Interconnect and substrate modeling and extraction
- 10.4 High-frequency and electromagnetic simulation of circuits
- 10.5 Thermal and electrothermal simulation

11. Timing Analysis and Design for Manufacturability

- 11.1 Design for yield, defect tolerance, cost issues, and impacts of DFM
- 11.2 Process technology development, characterization, and modeling
- 11.3 Deterministic static timing analysis and verification
- 11.4 Statistical performance analysis and optimization
- 11.5 Design for resilience under manufacturing variations

12. Physical Design and Manufacturability

- 12.1 Physical floorplanning, partitioning, placement
- 12.2 Buffer insertion, routing, interconnect planning
- 12.3 Physical verification and design rule checking
- 12.4 Automated synthesis of clock networks
- 12.5 Reticle enhancement, lithography-related design optimizations

13. Signal Integrity and Design Reliability

- 13.1 Signal integrity, capacitive and inductive crosstalk
- 13.2 Reliability modeling and analysis
- 13.3 Novel clocking and power delivery schemes
- 13.4 Power grid robustness analysis and optimization
- 13.5 Soft-errors and single-event upsets (SEUs)

14. Analog/Mixed-Signal and RF

- 14.1 Analog, mixed-signal, and RF design methodologies
- 14.2 Automated synthesis and macromodeling
- 14.3 Analog, mixed-signal and RF simulation and optimization

15. FPGA Design Tools and Applications

- 15.1 Rapid prototyping
- 15.2 Logical synthesis and physical design techniques for FPGAs
- 15.3 Configurable and reconfigurable computing

16. Testing

- 16.1 Test quality and reliability, nanometer technology test, current-based test
- 16.2 Digital fault modeling, automatic test pattern generation
- 16.3 Digital design-for-test, test data compression, built-in self test
- 16.4 Memory test and repair, FPGA testing
- 16.5 Fault tolerance and on-line testing
- 16.6 Analog/mixed-signal/RF testing
- 16.7 Board- and system-level test
- 16.8 Silicon debug, post-silicon design validation

17. New, Emerging, or Specialized Design Technologies, including but not restricted to

- 17.1 MEMS, sensors, actuators, imaging devices
- 17.2 Nano-technologies, nano-wires, nano-tubes
- 17.3 Quantum computing
- 17.4 Biologically based or biologically inspired systems
- 17.5 New transistor structures and devices, new or radical process technologies

18. Special Theme Topic: Automotive Electronics

- 18.1 Safety critical systems design: engine control, brake systems, automated highways, security systems, low tire pressure monitors, traction control, and auto distance cruise control
- 18.2 Bus selection and verification challenges for LIN, CAN and FlexRay
- 18.3 Automotive convenience factors: control systems, entertainment, communication, navigation, climate control, rain sensing, active noise cancellation, and vehicle stability
- 18.4 Analog mixed-signal design challenges
- 18.5 Automotive as an EDA driver: will automotive define ESL for EDA?
- 18.6 Issues with FPGA, ASIC and ASSP based design

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REGULAR PAPERS DUE BEFORE 5 pm MST, Nov. 20, 2006

Regular paper submissions MUST (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) MUST NOT include name(s) or affiliation(s) of the author(s) anywhere on the manuscript or abstract, and any references to the author(s) own previous work or affiliations in the bibliographic citations must be in the third person. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously under review by another conference, will be rejected. DAC will work cooperatively with other conferences and symposia in the field to check for double submissions. Additional submission guidelines are available on the DAC website (after September 1, 2006). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Notice of acceptance will be sent via email by March 9, 2007.

SPECIAL SESSIONS DUE BEFORE 5 pm MST, Nov. 1, 2006

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

PANELS and TUTORIALS DUE BEFORE 5 pm MST, Nov. 1, 2006

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panel and tutorial proposals.

STUDENT DESIGN CONTEST DUE BEFORE 5 pm MST, Dec. 6, 2006

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Three categories of designs - operational, system and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation and test plan is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2005. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2007). Additional contest rules are available on the DAC web site.

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