# PROCEEDINGS 2005

## DESIGN AUTOMATION CONFERENCE


## Anaheim Convention Center
## Anaheim, CA June 13-17, 2005

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ACM SIGDA special interest group on design automation

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# GENERAL CHAIR'S WELCOME

Welcome to the 42nd Design Automation Conference and the city of Anaheim! More than ever, DAC is the place where researchers and developers, industry and academia, exhibitors and their customers come to learn about the latest breakthroughs, the latest products, and the latest business deals in electronic design automation.

In addition to the industry luminaries and the best and the brightest innovators, DAC has the highest density of customers who make buying decisions of any similar conference. The thousands of attendees – system and chip designers, tool developers, analysts, executives, faculty, and students – are a diverse group who make DAC the place to be, the one place to meet your customers and suppliers, your colleagues and competitors, your former students, employees, and managers! You will find others with common interests and concerns, learn about new ideas in the technical sessions and new products on the exhibit floor, and get a view of trends, challenges, and solutions in electronic design automation. Your participation is limited only by your time and stamina.

This year's Tuesday keynote speaker is Bernard S. Meyerson, IBM Fellow, Vice President, and Chief Technologist of IBM's Systems and Technology Group, who will discuss the direction of design as scaling ends. Dr. Meyerson was named by EE Times as one of thirteen people "who are influencing the course of semiconductor development technology and taking it into realms that exceed the bounds set by the inventors of the transistor more than fifty years ago." On Thursday, Ronald A. Rohrer, Wilkoff Chair University Professor Emeritus of Electrical and Computer Engineering at Carnegie Mellon University and a design automation entrepreneur, will discuss innovation in the EDA industry. Dr. Rohrer is a winner of the EDA Consortium Phil Kaufman Award and Corporate Vice President, Advanced Research and Development, Cadence Design Systems, Inc.

The technical program this year was selected from 735 submissions, and the 74 members of the Technical Program Committee had to make difficult choices. The committee has produced a diverse technical program consisting of 154 papers in 40 sessions, plus nine special sessions and eight panels. The Panel Committee has put together these exciting panels as well as 18 events in the DAC Pavilion on the exhibit floor. The week is complemented by six tutorials on timely topics on Monday and Friday. System-level design, design for manufacturability, power reduction, and verification – problems old and new – form the core of the technical program.

This year, in addition to Management Day on Tuesday, is DAC's first theme day, Wireless Wednesday, with a range of technical talks and panels, discussion on the exhibit floor in the DAC Pavilion, and the showcasing of wireless products and applications. The exhibit floor, using the integrated booth/suite layout introduced successfully last year, features over 230 companies, with 50 new exhibitors. The excitement of the DAC Pavilion, Monday's Happy Hour, and a "Wireless Walk" highlighting tools and applications, and, of course, the latest products, make the exhibits a key part of the conference.

The efforts of many people go into making DAC the success it has been for over forty years as the premier design automation event for the entire community. The authors, speakers, and session chairs; the reviewers, session organizers, moderators, and panelists; the members of the DAC Executive Committee, Technical Program Committee, and Exhibitor Liaison Committee, all volunteers, deserve special thanks. MP Associates, Inc., conference and exhibit managers, continue to be unwaveringly focused on DAC's success. We are grateful for the support of our sponsors, ACM/SIGDA, IEEE/CASS/CANDE, and the EDA Consortium, and for the technical cooperation of the IEEE Solid State Circuits Society.

And special thanks to you, the DAC attendees. We wish you a productive and exciting week at DAC!

**William H. Joyner, Jr**
*General Chair*
42nd Design Automation Conference

# PROCEEDING OF THE 42ND DESIGN AUTOMATION CONFERENCE®

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Chair: Wanda Gass *(Texas Instruments, Inc.)*
Organizer: Wanda Gass



## SESSION 34: Architectural Support for Communication

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Organizers: Marcello Coppola, Peter Marwedel



## SESSION 35: New Approaches to Physical Design Problems

Chair: Chung-Kuan Cheng *(University of California)*
Organizers: Louis Scheffer, Malgorzata Marek-Sadowska

## SESSION 55: Reduced-Order Modeling

Chair: Janet Wang Roveda *(University of Arizona)*
Organizers: Byron Krauter, Vikram Jandhyala

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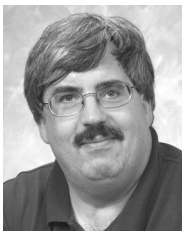

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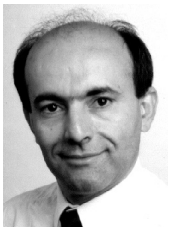

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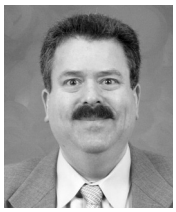

**Bernard S. Meyerson**
IBM Fellow, Vice President, & Chief Technologist
*IBM Systems and Technology Group*
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## How Does One Define "Technology" Now That Classical Scaling Is Dead (and Has Been for Years)?

Abstract: Over the past four decades, the IT industry has relied upon the classical scaling of semiconductor technology to drive both performance and product economics. Often confused with Moore's Law, classical scaling speaks to the science driving performance gains over the past decades, not the subset economic issue addressing the areal density of transistors on a chip. In effect, classical scaling had been the "glue" binding microprocessor economics, as stated by Moore's Law, to expectations for ongoing progress in microprocessor performance. The impact of the loss of that linkage with the demise of classical scaling has yet to be fully comprehended.

The discontinuity engendered by the failure of classical scaling has shaken the microprocessor and IT industry to its foundation, forcing radical shifts in product roadmaps and business focus for those unprepared. This talk will briefly review the origins of this discontinuity, but more critically emphasize new strategies, such as Holistic Design, as employed to drive continued progress in IT performance. First results of the movement to Holistic Design at chip and system level will be reviewed, as will strategies meant to accelerate efforts in this vein.

Biography: Bernard S. Meyerson is Chief Technologist and Vice President, Technology, for IBM's Systems and Technology Group. He joined IBM Research in 1980, and led the development of silicon germanium and other high-performance mixed-signal technologies over a period of ten years, and subsequently led several large organizations within IBM focused on the development of communications technology, spanning the range from pervasive wireless enablement to high-end data transport. Dr. Meyerson currently leads IBM's Semiconductor Research and Development Center, the multi-company technology alliance located at IBM's East Fishkill semiconductor facility.

Dr. Meyerson was named IBM Fellow, the company's highest technical honor, in 1992. He is a Fellow of the American Physical Society and the IEEE and a recipient of the Materials Research Society Medal, the Electrochemical Society Electronics Division Award, the 1999 IEEE Ernst Weber Award for the body of work culminating in the commercialization of Si-Ge-based communications technology, and the IEEE Electron Devices Society J. J. Ebers Award. He was cited as "Inventor of the Year" in 1997 by the New York State Legislature, and was honored as the 1999 "United States Distinguished Inventor of the Year" by the U.S. Patent and Trademark Office. In 2002, he was elected to the National Academy of Engineering, and in 2003, he was named by EE Times as one of thirteen people "who are influencing the course of semiconductor development technology and taking it into realms that exceed the bounds set by the inventors of the transistor more than fifty years ago." He holds a Ph.D. in physics from City College of the City Universtity of New York.

# THURSDAY KEYNOTE ADDRESS

**Ronald A. Rohrer**
Corporate Vice President,
*Advanced Research and Development*
*Cadence Design Systems*

## Innovation in the EDA Business Need Not Be an Oxymoron

Abstract: Innovation in EDA is often thought to happen in an isolated *eureka* moment experienced by a *superstar*. As many of us have found out the hard way, such events are all too rare, and in any case do not create business success. People with a common goal and passion often together share the breakthrough ideas and their results. To sustain the level of innovation for EDA to survive, we should first recognize that it is a team effort, and then that potential breakthroughs and even just necessary progress can be part of a managed process. A renewable model for EDA innovation that is proving successful involves five steps in progression: problem to prototype, to partnership, to product and, finally, to proliferation.

Biography: Ron A. Rohrer has been affiliated with EDA in various capacities - in semiconductor and software companies, in start-ups and established companies, in universities and in venture capital - for more than forty years. As would anyone having spent so much time in and around EDA, he has seen, learned, accomplished ... and endured a lot. His passion for teamwork to achieve research, development, and business success has been evident throughout his career. Presently he is with Cadence, working as part of an RF IC EDA advanced research and development team.

Dr. Rohrer is a Fellow of the IEEE and a recipient of the IEEE Education Medal, the SRC Technical Excellence Award, the 1996 NEC Computer and Communication Prize, and the Electronic Design Automation Consortium 2002 Phil Kaufman Award. He was elected to the National Academy of Engineering in 1989 for his contributions to circuit simulation that have enabled deep submicron IC design. He started his industrial career at Fairchild Semiconductor and has served as technical consultant and advisor to many leading EDA and electronics companies. Dr. Rohrer has taught at the University of Illinois at Urbana-Champaign, Southern Methodist University, the University of California at Berkeley, and Carnegie Mellon University, where he is professor emeritus of electrical and computer engineering. An entrepreneur, he was founder of Performance Signal Integrity (later acquired by Integrated Silicon Systems and merged with ArcSys to form Avant! Corporation) and was chairman of Neolinear before its acquisition by Cadence. He holds an S.B. from MIT and a Ph.D. in electrical engineering from the University of California at Berkeley.

## Marie R. Pistilli Women in EDA Achievement Award

**Kathryn Kranen** - President & CEO, *Jasper Design Automation,* Mountain View, CA
For her significant contributions in helping women advance in the field of EDA technology.

## The P. O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P. O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under represented groups (women, African American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship, and SIGDA continues to administer the program for DAC. DAC normally funds two or more $4000 scholarships, renewable up to 5 years, to graduating high school seniors.

The 2005 winners are:

**Elizabeth Hong-An Boi Ha -** attending Georgia Institute of Technology

**Hans Edgar Anderson -** attending Massachusetts Institute of Technology

For more information about the P. O. Pistilli scholarship, contact Dr. Cherrice Traver, ECE Dept., Union College, Schenectady, NY 12308. email: traverc@union.edu

## Design Automation Conference Graduate Scholarships

Each year the Design Automation Conference sponsors several $24,000 scholarships to support graduate research and study in Design Automation (DA), with emphasis in "design and test automation of electronic and computer systems." Each scholarship is awarded directly to a university for the Faculty Investigator to expend in direct support of one or more DA graduate students.

The criteria for granting such a scholarship expanded in 1996 to include financial need. The criteria are the academic credentials of the student(s); the quality and applicability of the proposed research; the impact of the award on the DA program at the institution; and financial need. Preference is given to institutions that are trying to establish new DA research programs.

Prof. **Elias Kougianos**, Dept. of Engineering Technology, *University of North Texas,* Denton, TX

Student: **Rahul Allawadhi**

*The SPICE Modernization Project*

Prof. **Yehia Massoud**, Dept. of Electrical and Computer Engineering, *Rice University,* Houston, TX

Student: **Arthur Nieuwouldt**

*Spiral Inductor Synthesis for Mixed-Signal Systems*

Information on next year's DAC scholarship award program will be available on the DAC web site: http://www.dac.com.

## DAC/ISSCC 2005 Student Design Contest Winners

**Operational Category:**

**1st Place** *A 50MS/s (35mW) to 1kS/s (15uW) Power Scaleable 10b Pipelined ADC with Minimal Bias Current Variation*

**(Best Overall)** Imran Ahmed, David Johns – *University of Toronto,* Toronto, ON, Canada

**2nd Place** *A 1.3 TOPS H.264/AVC Single-Chip Encoder for HDTV Applications*
Tung-Chien Chen, Yu-Wen Huang, Chen-Han Tsai, To-Wei Chen, Ching-Yeh Chen, Liang-Gee Chen – *National Taiwan University,* Taipei, Taiwan

**3rd Place** *A Side-Channel Leakage Free Coprocessor IC in 0.18 µm CMOS for Embedded AES-based Cryptographic and Biometric Processing*
Kris Tiri, David Hwang, Alireza Hodjat, Bo-Cheng Lai, Shenglin Yang, Patrick Schaumont, Ingrid Verbauwhede – *University of California,* Los Angeles, CA

**Conceptual Category:**

**1st Place** *Design and Implementation of a Fractional-N Frequency Synthesizer for Cellular Systems*
Petrus J. Venter, Saurabh Sinha – *University of Pretoria,* Pretoria, South Africa

**2nd Place** *A 1-V IEEE 802.11a/b/g-Compliant Receiver IF-to-Baseband Chip in 0.35 µm CMOS for Low-Cost Wireless SiP*
Pui-In Mak, Rui P. Martins – *University of Macau,* Macao SAR, China; Seng-Pan U – *Chipidea Microelectronics (Macau) Ltd.,* Macao SAR, China

**3rd Place** *Collision Detection System using an FPGA Implemented on the FPX Platform*
Hasan N. Atay, Burchan Bayazit, John W. Lockwood – *Washington University,* St. Louis, MO

## ACM Transaction on Design Automation of Electronic Systems (TODAES) 2005 Best Paper Award

*Technology Mapping and Architecture Evaluation for k/m-macrocell-based FPGAs*

Volume 10, No. 1, January 2005, Pages: 3 - 23.

**Jason Cong** - *University of California,* Los Angeles, CA
**Hui Huang** - *Sun Microsystems,* Santa Clara, CA
**Xin Yuan** - *IBM Corp.,* Essex Junction, VT

## The Association for Computing Machinery/Special Interest Group on Design Automation (ACM/SIGDA) presents its Distinguished Service Award

**Mary Jane Irwin** - *Penn State University,* University Park, PA
For dedicated service as Editor in Chief of ACM TODAES (1998 - 2004), and many years of service to SIGDA, DAC, and the EDA profession.

## 2004 Phil Kaufman Award for Distinguished Contributions to EDA

**Joe Costello** - *Chairman & CEO of think3, Inc. and former Chairman & CEO of Cadence Design Systems, Inc.*
Mr. Costello was selected to receive the 2004 Phil Kaufman Award because of his business contributions that helped grow the EDA industry. Under his leadership (1987-1997), Cadence became the world's leading supplier of EDA software and services, and one of the top ten largest software suppliers in the world.

## IEEE Circuits and Systems Society
## 2005 VLSI Transactions Best Paper Award

**Radu Marculescu** - *Carnegie Mellon University,* Pittsburgh, PA
**Girish Varatkar** - *Carnegie Mellon University,* Pittsburgh, PA
For the paper entitled, *On-Chip Traffic Modeling and Synthesis for MPEG-2 Video Applications,* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 1, pp. 108-119, January 2004

## IEEE Circuits and Systems Society 2005 Darlington Award

**Payam Heydari** - *University of California,* Irvine, CA
For the paper entitled, *Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise*, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 12, pp. 2404-2416, December 2004

## IEEE Circuits and Systems Society 2005 Industrial Pioneer Award

**Yervant Zorian** - *Virage Logic Corp.,* Freemont, CA
For his contributions to design for test technology through Built-In Self-Test solutions and design tools that dramatically boosted the quality and reliability of digital systems and the efficiency of design and test engineers.

## IEEE Circuits and Systems Society
## 2005 Outstanding Young Author Award

**Chris Hyung-Il Kim** - *Purdue University,* West Lafayette, IN
For the paper entitled, *Ultra Low-Power DLMS Adaptive Filter for Hearing Aid Applications*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 11, no. 6, pp. 1058-1067, December 2003 (with H. Soeleman and K. Roy)

## IEEE Circuits and Systems Society 2005 Donald O. Pederson Award

**Subhasish Mitra** - *Intel Corp.,* Folsom, CA
**Kee Sup Kim** - *Intel Corp.,* Sacramento, CA
For the paper entitled, *X-compact: An Efficient Response Compaction Technique*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 3, pp. 421-432, March 2004

## 2005 IEEE Fellows

**Fadi Joseph Kurdahi** - *University of California,* Irvine, CA
For contributions to design automation of digital systems and to reconfigurable computing.

**David J. Comer** - *Brigham Young University,* Provo, UT
For leadership in engineering education and publication of electronic circuit design textbooks.

**Kartikeya Mayaram** - *Oregon State University,* Corvallis, OR
For contributions to coupled device and circuit simulation.

**Chandu Visweswariah** - *IBM Corp.,* Yorktown Heights, NY
For contributions to large scale integrated circuits.

**Reinaldo Alvarenga Bergamaschi** - *IBM Corp.,* Yorktown Heights, NY
For contributions to the development system design tools and methodologies.

**Domine Leenaerts** - *Phillips Research,* Eindhoven, Netherlands
For contributions to nonlinear circuit theory and design.

# REVIEWERS

A total of 735 manuscripts were submitted to the 42nd DAC. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts and returned the review forms completed. Our thanks to all of those who participated and contributed to the success of the Conference.

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DAC is the premier conference devoted to Design Automation (DA) and the application of DA tools in designing electronic systems. Four types of submissions are invited: regular papers, special topic sessions, panels, and tutorials. Submissions must be made electronically at www.dac.com. Panel and Tutorial suggestions and Special Session submissions are due **NO later than 5:00 pm MST, November 2, 2005**; Regular Papers are due **NO later than 5:00 pm MST, December 19, 2005.**

## TOPICS OF INTEREST

DAC 2006 is seeking papers that deal with design tools, design methods and case studies, and embedded design in a number of categories described below.

**Design Tools** papers describe contributions to the research and development of design tools and their supporting algorithms.

**Design Methods** and case studies papers describe innovative methodologies for the design of electronic circuits and systems, as well as creative experiences with design automation in state-of-the-art design projects.

**Embedded Systems** are characterized by mixed hardware and software components with limited resources. Increases in software content introduce new system design issues. Embedded design papers describe tools, methods, and case studies for applications with specific embedded system content.

Submitters no longer need to specify a tools, methods, or embedded systems track, but only specify a category from the 18 listed below.

**Categories:**

**1. Circuit Simulation and Timing Analysis**
- Electrical-level circuit and timing simulation
- Static timing analysis and timing verification
- Electrothermal simulation methods

**2. Design-for-Manufacturability**
- Design for yield, cost issues, and impacts of DFM
- Process technology development, extraction, measurement, and modeling
- Statistical performance analysis and optimization
- Reticle enhancement, lithography-related design optimizations

**3. Power Analysis and Low-Power Design**
- Analysis and estimation of power
- Embedded low-power approaches: partitioning, scheduling, and resource management
- Device, circuit, and system techniques for low-power design
- Impacts on thermal management of low-power design techniques

**4. Testing**
- Digital, system, memory, analog/mixed-signal, and RF test
- ATPG, fault modeling, DFT and BIST, test debugging
- Scan-based testing, delay testing, on-line testing
- Cost issues and impacts of testability

**5. Verification**
- Functional, transaction-level, RTL and gate-level modeling and verification of hardware design
- Dynamic simulation, equivalence checking, formal (and semi-formal) verification model and property checking
- Emulation and hardware simulators or accelerator engines
- Modeling languages and related formalisms, verification plan development and implementation
- Assertion-based verification, coverage-analysis, constrained-random testbench generation

**6. IC Physical Design**
- Physical floorplanning, partitioning, placement
- Buffer insertion, routing, interconnect planning
- Module generation, cell sizing, and library optimization
- Physical verification

**7. Logic Synthesis**
- Combinational, sequential, and asynchronous logic synthesis, both technology-independent and dependent
- Library mapping, cell-based design and optimization
- Transistor sizing
- Interactions between logic design and layout or physical synthesis

**8. High-Level Synthesis**
- High-level, behavioral, algorithmic, and architectural synthesis, "C" to gates tools and methods
- HW-SW interface synthesis, communication and network synthesis
- Synthesis of digital circuits above the RTL level
- Resource scheduling, allocation, and synthesis

**9. Interconnect**
- Interconnect modeling and extraction for current and advanced mainstream IC processes
- Model-order reduction methods for linear systems
- Substrate modeling with interconnect parasitic extraction
- High-frequency and electromagnetic simulation of circuits

**10. Signal Integrity and Design Reliability**
- Signal integrity, thermal analysis, and reliability modeling and analysis
- Timing, clocking, and power distribution, especially novel techniques
- Power grid robustness analysis and optimization
- Capacitive and inductive crosstalk noise
- Soft-errors and single-event upsets (SEUs)

**11. Analog/Mixed-Signal and RF**
- Analog, mixed-signal, and RF design
- Automated synthesis and macromodeling
- Simulation and optimization

**12. FPGA Design Tools and Applications**
- Rapid prototyping
- Logical synthesis and physical design techniques for FPGAs
- Configurable and reconfigurable computing

**13. Embedded HW Design and Applications**
- Case studies of embedded system design
- Flows and methods for specific applications and design domains

**14. Embedded SW Tools and Design**
- Retargetable compilation
- Memory/cache optimization
- Real-time single- and multi-processor scheduling, linking, loading
- Real-time operating systems

**15. System-Level Design and Co-Design**
- System specification, modeling, simulation, and performance analysis
- Scheduling, HW-SW partitioning
- IP and platform-based design, IP protection
- Communications-based design
- System-on-Chip (SoC), Network-on-Chip (NoC), Multi-processor SoC (MPSOC)
- Application-specific processor design tools

**16. New, Emerging, or Specialized Design Technologies Including, but Not Restricted to**
- MEMS, sensors, actuators, imaging devices
- Nano-technologies, nano-wires, nano-tubes
- Quantum computing
- Biologically based systems
- New transistor structures and devices, new or radical process technologies

**17. Beyond Die-Integration and Packaging**
- Chip-package-board codesign
- System-in-Package
- 3D design, stacked devices
- Analysis and optimization (signal integrity, physical layout, simulation) beyond the die

**18. Special Theme Day—ENTERTAINMENT, GAMES, and MULTIMEDIA**
- Design issues pertaining to mobile devices, music, video, broadcast, video on demand, and other multimedia/consumer entertainment devices
- Intensive multimedia processing as part of entertainment computing and specialized entertainment engine design
- Design and implementation of game playing, video, and audio engines
- Cross-platform entertainment and game software design and design implications
- System-level design approaches for games and multimedia entertainment devices

**ALL SUBMISSIONS MUST BE MADE ELECTRONICALLY AT THE DAC WEB SITE: WWW.DAC.COM**

## REGULAR PAPERS DUE BEFORE 5 pm MST, Dec. 19, 2005

Regular paper submissions must (1) be in PDF format only, (2) contain an abstract of approximately 60 words clearly stating the significant contribution, impact, and results of the submission, (3) be no more than 6 pages (including the abstract, figures, tables, and references), double columned, 9pt or 10pt font, and (4) **MUST NOT** include name(s) or affiliation(s) of the author(s) anywhere on the manuscript, abstract, or bibliographic citations. Format templates are available on the DAC web site for your convenience, but are not required. Submissions not adhering to these rules, or those previously published or simultaneously submitted to another conference, will be rejected. Additional submission guidelines are available on the DAC website (after Sept. 1, 2005). All regular papers will be reviewed as finished papers. Preliminary submissions will be at a disadvantage. Authors of accepted papers must sign a copyright release form for their paper. Notice of acceptance will be sent via email by April 17, 2006.

## SPECIAL SESSIONS DUE BEFORE 5 pm MST, Nov. 2, 2005

Special session submissions must include descriptions of suggested papers and speakers, and the importance of the special session to the DAC audience. DAC reserves the right to restructure all special sessions.

## PANELS and TUTORIALS DUE BEFORE 5 pm MST, Nov. 2, 2005

Panel and tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Tutorial suggestions must include a bulleted outline of covered topics. DAC reserves the right to restructure all panels and tutorials.

## STUDENT DESIGN CONTEST DUE BEFORE 5 pm MST, Dec. 6, 2005

Students are invited to submit descriptions of original electronic designs, either circuit level or system level. Student Design Contest paper submissions must (1) be in PDF format only, (2) contain the title of the project, (3) contain an abstract of approximately 60 words, (4) contain a complete description of the project, and (5) be no more than 6 pages (including the abstract, maximum of 10 figures/tables and references), double-columned, 9pt or 10pt font. The submission should clarify the originality, distinguishing features, and measured performance of the design. Two categories of designs - operational and conceptual - are eligible for awards. For operational designs, proof-of-implementation is required, while for conceptual designs, complete simulation is necessary. Designs must have taken place as part of the students' work at the university and must have been completed after June 2004. Submitted designs should not have received awards in other contests. Selected designs will be presented at the conference (and at ISSCC in February 2006). Additional submission guidelines are available on the DAC web site.

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