Research Network for System Level Design of Embedded Systems: Dynamic Memory Allocation Design Flow Case Study

Stylianos Mamagkakis[1, 3], David Atienza[2], Francky Catthoor[3], Dimitrios Soudris[1] and Jose M. Mendias[2]

[1] *VLSI Design Center- Democritus Univ. of Thrace 67100 Xanthi, Greece {smamagka,dsoudris} @ee.duth.gr*

[2] *DACYA, Univ. Complutense de Madrid 28040 Madrid, Spain {datienza,mendias} @dacya.ucm.es*

[3] *Interuniversity Micro-Electronics Centre (IMEC vzw) 3001 Heverlee, Belgium {mamagka,catthoor} @imec.be*

Abstract

The challenges encountered in system level design require a global approach and considerable manpower, which are not likely to be found in a single organization. Cooperation and sophisticated communication between partners from both academia and industry are required. This paper describes the formal relationship and collaboration between IMEC and several Universities for research and training in the domain of system level design in embedded systems. IMEC (Leuven, Belgium) provides a meeting point between multiple academic institutions and a gateway to relevant information and drivers from the industry, unifying the common research goals of several academic groups working in this area in a consistent flow, sensitive to the market needs. In this paper we focus in the general concept of the cooperation network, which can be illustrated shortly by one part of it, namely the dynamic memory allocation issues of the design flow and the related universities in this effort: DUTH (Xanthi, Greece) and DACYA UCM (Madrid, Spain).

1. Introduction

The collaboration illustrated in this paper addresses the needs for a unified, consistent global approach to the various problems encountered in embedded system design. These problems are so closely interconnected that it is common to worsen one aspect of the embedded system design, while trying to improve another [1]. In fact, a small research group with limited resources will ignore the global view in order to maximize its potential within its limited research focus. In order to realize a global approach, without sacrificing quality, a network of research groups is needed. It should be guided by a coordinator that has sufficient critical mass and has access to the necessary information to work on practically relevant end goals.

IMEC with its unique balance between academic and industrial R&D can lead this effort of a star-shaped training and research network. Its geographical location in Belgium offers a unique meeting point for researchers of universities all across Europe, where they can be trained and establish a collaboration towards interconnected goals in embedded system design. The context of the collaboration focuses mostly on the mapping of concurrent, dynamic applications, which are increasingly important in multimedia and network applications. Several design steps are required to cost-effectively map the data and tasks in such applications to a multi-processor platform.

2. Dynamic Memory Allocation Design Flow Case Study

Modern embedded applications have become increasingly dynamic and consist of multiple tasks, which run in multi-processor embedded systems. Design optimizations at the system level are required to optimize the energy consumption, memory footprint, memory accesses and execution time of the final design [1]. A complete optimization design framework is proposed by IMEC in collaboration with its university partners at the system level (see Figure 1), which can be followed in a step-by-step procedure. Each stage consists of systematic design methodologies (or steps), which are closely interconnected and the outputs of the higher ones pass their constraints to the lower ones (more details about the optimization steps and the way they are derived can be found in [2]).

These systematic methodologies require many person-years of research to be developed and perfected and different research networks are assembled in order to take advantage of the expertise of the individual researchers that comprise them. In fact, the proposed system level methodology comprises the combined effort of 14 PhD students and 7 professors from IMEC, the Democritus

University of Thrace (DUTH located in Xanthi, Greece) and the Department Arquitectura de Computadores y Automatica (DACYA UCM located in Madrid, Spain), as shown in Figure 2. Earlier on, also ESAT (K.U. Leuven, Belgium) and recently also U. Bologna have become evolved (see Sect. 4).

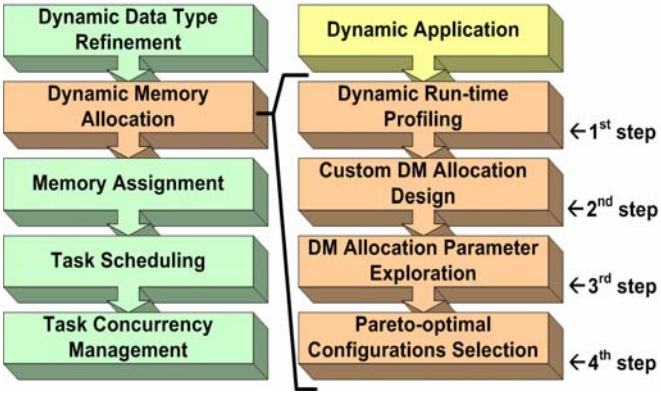

Fig.1. System level design optimization steps and dynamic memory allocation sub-steps

As shown in Fig. 1, the transformation and refinement of the original dynamic data types in the specification are addressed. The transformation and refinement of the original dynamic data types in the specification are addressed. IMEC focuses its efforts both on dynamic multimedia applications, e.g. scalable video coding, dynamic image processing, video games, graphical user interface with animation of rendered multimedia objects, as on wireless network applications. In both cases, the target is to embed them on a cost/power-sensitive platform. In these applications, the conventional compile-time techniques only allow to come up with static solutions that assume worst-case and hence much too pessimistic requirements on memory footprint and performance. Hence, the data type transformation methodology was further developed and extended to generate a low cost implementation in terms of performance, memory footprint and energy consumption, which is especially suited for portable appliances, involving dynamic data types. Trade-offs up to several orders of magnitude have been obtained for realistic applications. Also an effective prototype tool has been completed to automatically profile the evolving dynamic memory behavior of the application and adding a systematic exploration technique was started. This research has happened in cooperation with the Univ. Compl. of Madrid and Democr. Univ. Thrace. It builds further on the past experience in the Matisse research project for wired telecom protocols.

The refined dynamic data types still have to be (de)allocated in the virtual memory space and this typically happens with a dynamic memory manager. The dynamic memory manager is analyzed separately on the right side of Fig. 1. In this case, standard library based solutions lead to much access and footprint overhead compared to the minimal achievable costs. Hence, we have further extended our techniques to fully automatically explore cost-efficient custom dynamic-memory manager solutions exploring still the complete search space in a systematic way, including now also the total energy consumption as an overall objective on top of the ones for memory accesses and footprint. All this is based on a detailed analysis of the (de)allocated patterns of the application. Compared with conventional (dynamic) memory management techniques for embedded systems, IMEC has obtained significant gains, both for multi-media applications and for wireless networks. A tool has been developed that supports the complete trajectory, starting from C++ source code.

The performance and energy consumption of the shared memory hierarchy on a platform depends largely on how the data access of a dynamic application is ordered and assigned to the physically available memories. Therefore, IMEC has developed new techniques to solve the data-to-memory assignment problem for multi-tasked applications where data of dynamically created/deleted tasks is allocated at runtime. In contrast to the previous years where focus was mainly on memory access scheduling and assignment, work now started on a complete script for task-level data transfer and storage exploration. For this purpose a representative application and target platform were selected, and the different steps were evaluated that are required to bridge the gap between the high-level object-oriented specification of data in dynamic concurrent types, together with their realization on a distributed hierarchical memory organization. We are also investigating the use of a hardware emulation platform to evaluate the mappings. This research was executed in cooperation with the Univ. Complutense Madrid, Univ. of Bologna, and Univ. Barcelona.

To show the productivity of such combined approach, just in the dynamic memory allocation step, the cooperative work of 3 to 4 PhD candidates from each research group working full-time during the last 3 years for the development of the dynamic memory allocation methodologies have accomplished the development of 4 national and European funded research projects and the publication of 4 internal technical reports, 21 conference papers, 4 journal papers and 1 book chapter.

3. IMEC – Universities Network

The network between the research groups in IMEC and in the universities was star-shaped up to now. This means that the formal relationship is between any given university and IMEC and not yet between the universities themselves. The typical research work plan involves regular visits of at least one researcher of each group to IMEC for a period of 3 to 6 months per year. Researchers working in the

same optimization step have to overlap for at least 3 months each year to synchronize with each other properly.

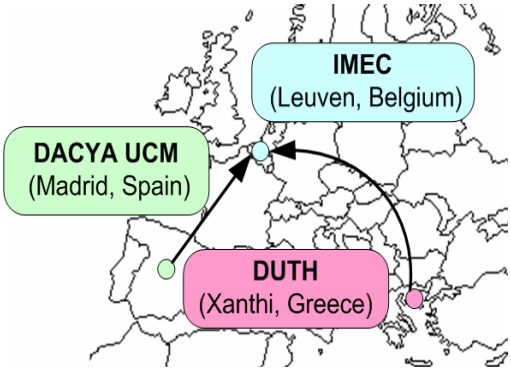

Fig. 2. IMEC-Universities network for embedded system design

In the case of the research and training required for the optimization step of dynamic memory allocation, one PhD candidate from DUTH and one from DACYA UCM have spent 20 and 21 months respectively in IMEC in the last 3 years. The economic support for the travel and cost of living abroad at this stage is largely provided by EU-funded Marie Curie Fellowships [4].

The EU-funded Marie Curie Fellowships are not tied to other specific projects (e.g., IST or national projects) but are a project on itself. The money that the PhD candidates receive are on addition to their existing funds and are provided in order to pay for their travel costs, their accommodation and living expenses in the country where their host institution is (i.e., in this case IMEC, Leuven).

During their stay in IMEC, the researchers (mainly PhD students) follow general training courses (e.g. "Speaking in public" and "Writing technical reports") and more specialized courses on the unified meta-design flow concepts [1], which are a basis for the global approach of system design. Additionally, they follow specialized courses on the latest system design flows, design toolkits and improvement methodologies.

Finally, they enjoy a high quality research environment (both in facilities and research personnel) and are given the attractive opportunity to interact with both the industrial and the academic international world. Also, this includes seminars once every week from prominent industry and academic figures in the IMEC auditorium.

During each visit, the researchers from the universities collaborate also with the corresponding researchers in IMEC (which work on dynamic memory allocation in this particular case study) and define the interactions between the steps with researchers working in other optimization steps. Most importantly, in each visit in IMEC they kick start the research of one systematic methodology (step) of the dynamic memory allocation and then they continue their research on this step, when they return in their research group back in their university. For the rest of the year, they retain their strong cooperation by e-mail, web conferencing and phone-conference calls.

The PhD candidates also coordinate the effort within their research groups devoted to the same research goal. The research done locally in each university is supported by funds from the corresponding laboratory acquired through associated research projects or research grants. These research projects are not directly related to the Marie-Curie fellowships but are related to the type of research that is done during the fellowships in the host institution (e.g. see AMDREL project [5]).

4. Conclusions and Future Prospects

The research network addressed in this paper, has been very successful in the field of dynamic memory allocation and system level design for embedded systems and already 2 students (i.e. M. Leeman and D. Atienza) have received their PhDs, while working in the network environment. This collaboration is and will be continued and extended in the future to other research topics. Finally, a polyhedron-shaped network between the current groups and additional excellent institutions in Europe, like DEIS University of Bologna and CS 12 of Dortmund, is under construction to ensure the best interaction and mobility between the partners. Further actions under the ARTIST2 [6] and HIPEAC [7] umbrella are also envisioned.

Acknowledgements

This work is partially supported by the E.C. funded program AMDREL IST-2001-34379, the Spanish Government Research Grant TIN2005-05619 and E.C. Marie Curie Fellowship contract HPMT-CT-2000-00031.

REFERENCES

[1] F. Catthoor et al., *"Unified meta-flow summary for low-power data-dominated applications"*, Kluwer Publications, 2000.

[2] *IMEC Design Technology Program*, http://www.imec.be/ovinter/static_research/designtechnology.shtml

[3] S. Mamagkakis et al., *"Energy-efficient dynamic memory allocators at the middleware level of embedded systems"*, in Proc. of EMSOFT, S. Korea, 2006

[4] *Marie Curie Actions - Human Resources and Mobility Activity*, http://europa.eu.int/comm/research/fp6/mariecurie-actions/action/fellow_en.html

[5] AMDREL project "Architectures and Methodologies for Dynamic REconfigurable Logic", http://vlsi.ee.duth.gr/amdrel/

[6] ARTIST 2, Network of Excellence on embedded system design, http://www.artist-embedded.org/artist/

[7] European Network of Excellence on High-Performance Embedded Architecture and Compilation, http://www.hipeac.net/