063174

THE UNIVERSITY of York

Degree Examinations 1999

DEPARTMENT OF COMPUTER SCIENCE

Real-Time Systems and Programming Languages

Time allowed: **Three (3) hours**

Candidates should answer not more than **four** questions

1 (25 marks)

(i) [9 marks] Describe briefly how

- processes are created in occam2
- processes are created in POSIX
- tasks are created in Ada 95

(ii) [6 marks] Discuss the merits of having concurrency defined by a programming language as opposed to having a sequential programming language and relying on operating system primitives for concurrency.

(iii) [10 marks] A particular operating system has a system call (*Run_Concurrently*) which takes an unconstrained array. Each element of the array is a pointer to a parameterless procedure. The system call executes all the procedures concurrently and returns when all have terminated.

Show how this system call can be implemented in Ada 95 using the Ada 95 tasking facilities. You may assume that the operating system and the application run in the same address space.

2 (25 marks)

(i) [15 marks] Define what is meant by **blocking time**. Compare and contrast the **original ceiling priority protocol** with the **immediate ceiling priority protocol** for single processor systems.

(ii) [10 marks] A program consists of five tasks, A,B,C,D,E (these are listed in priority order with A having the highest priority), and six resources R1, ... R6 (protected by semaphores implementing the Original Priority Ceiling Protocol). The resource accesses have worst-case execution times given in Table 1.

R1	R2	R3	R4	R5	R6
10ms	30ms	20ms	60ms	50ms	40ms

Table 1: Summary of the resources' execution requirements

Resources are used by the tasks according to Table 2.

Task	Uses
A	R3
B	R1,R2
C	R3,R4,R5
D	R1,R5,R6
E	R2,R6

Table 2: Summary of the tasks' resource requirements

Calculate the blocking time for each task in the above table.

3 (25 marks)

(i) [10 marks] Explain the facilities provided by the following occam2 primitive processes:

- ALT
- PRI ALT
- replicated ALT

(ii) [15 marks] A server process in occam2 receives synchronisation messages on the following channels.

```
CHAN OF ANY serviceA, serviceB, serviceC:
```

Write the body of the server process so that it performs all of the following operations.

- If client processes are waiting on all the channels, the server should service the clients in a cyclic order, that is, first a `serviceA` request, and then a `serviceB` request, and then a `serviceC` request, and then a `serviceA` request and so on.
- If not all channels have a client process waiting, the server should service the other channels in a cyclic order. The server should not suspend if there are clients still waiting for a service.
- If the server process has no waiting clients then it should NOT busy-wait; it should suspend waiting for any client request to be made.

4 (25 marks)

(i) [10 marks] Describe the facilities that Ada 95 has for programming device drivers.

(ii) [15 marks] The British government is concerned about the speed of cars using motorways. In the future, beacons will be set up at regular intervals along all motorways; they will continuously transmit the current speed limit. New cars will contain computers which will monitor the current speed limit and inform the driver when he/she exceeds the limit.

One car currently being designed (the Yorkmobile) already has the necessary hardware interfaces. They are as follows.

- Each car has a "speed control" 16 bit computer which has memory mapped I/O, with all I/O registers 16 bits in length.

- A register located at octal location 177760 interfaces to a device which monitors the road-side beacons. The register always contains the value of the last speed limit (in miles per hour) received from the road-side beacons.

- A pair of registers interface to an intelligent speedometer device which checks the speed of the car against a set limit. If the car goes faster than the set limit, the device generates an interrupt through octal location 60. The priority of the interrupt is 5. This interrupt is repeated every 5 seconds until the car is no longer speeding.

- The speedometer's register pair consists of a "control and status" register (CSR), and a "data buffer" register (DBR). The structure of CSR register is show in Table 3.

  The CSR register may be both read from and written to, and resides at address octal 177762.

  The DBR register is written to by the software. The value written represents a new speed limit (in miles per hour) to be checked by the speedometer. If this value falls outside the range 0 - 70 then an erroneous limit has been specified, and the device continues with the current limit. The address of the DBR register is octal 177764. The speedometer device generate an interrupt if the car exceeds the set speed limit or if the speed limit is erroneous.

Bits	Meaning
0	enable device
1	when set the value found in the DBR is used as the car's set speed limit
5 - 2	not used
6	interrupt enable
11 - 7	not used
15 - 12	error bits (0 = no error, >0 illegal limit)

Table 3: Control register structure speed computer

- A flashing light (on the car dashboard) can be turned on by writing to a register, located at octal address 177750, the value 1. The light will flash for 5 seconds only; the light will then be turned off automatically and the register reset to 0.

Design an Ada 95 device driver which will implement the following speed control algorithm.

Every 60 seconds the current speed limit should be read from the road-side beacon by the speed control computer. This value is to be passed unchecked to the speedometer device. If the car exceeds the limit then the dashboard light should be flashed until the car returns to the current limit or below the current limit.

5 (25 marks)

(i) [8 marks] What facilities does Ada 95 provide for manipulating time in a real-time program.

(ii) [5 marks] Briefly contrast the Ada 95 facilities for manipulating time with those provided by Real-Time Euclid and DPS.

(iii) [12 marks] Outline (with code) how Ada 95 supports sporadic tasks. How can the task protect itself from executing more often than its minimum inter-arrival time?

6 (25 marks)

(i) [4 marks] Explain the user needs for an asynchronous event handling mechanism.

(ii) [9 marks]

Describe the facilities provided by POSIX for asynchronous event handling at the PROCESS level.

(iii) [12 marks] A particular POSIX-based application consists of several periodic processes and has two modes of operation: MODE A and MODE B. The application has one process which only operates in MODE A. Sketch the design of this process assuming that when the system wishes to undertake a mode change, it sends a signal to all processes indicating the current mode of operation. Your answer can also assume the existence of a routine called WAIT_NEXT_PERIOD, which will suspend the process until its next period of execution is due. Note that a mode change should only effect the process at the beginning of each period.